100V/1.2A Non-synchronous Buck Converter with Ultra Low Quiescent Current

1 Descriptions

The ZCC10012 is a non-synchronous buck converterfeaturing a wide input voltage range of 6V to 100V, and is specifically optimized for applications demanding ultra-low standby power consumption. The converter can achieve high efficiency and can support up to 1.2A continuous load current with integrated Low RON high-side power MOSFETs. The ZCC10012 integrates a PG pin toindicate whether the output is within the target range, while for the ZCC10012, the PG pin is replaced by an EXTpin instead. The ZCC10012 can achieve much lowerstandby loss and higher light-load efficiency via the EXT tied to VOUT.

The device employs a constant on-time control mode which enables a fast transient response. It is compatible with low equivalent series resistance output capacitors such as polymer and ceramic (MLCC) capacitors with external compensation circuits.

The IC incorporates an internal VCC bias supply, which helps to eliminate the need for an external VCC capacitor and simplifies PCB layout.

The device supports protections including input under-voltage protection, cycle-by-cycle peak current limitation, short circuit protection with hiccup mode, and thermal shutdown protection with auto-recovery

ZCC10012 adopts SOP8 Package.

3 Applications

- High Voltage Post Regulator
- E-Bikes, Power and Garden Tools
- Motor Drivers, Drones, Telecom
- Industry Power Supplies

2 Features

- Wide VIN Range: 6V to 100V
- 10μA Ultra Low Quiescent Current
  - For ZCC10012: 3μA (The EXT pin is tied to VOUT)
- Up to 1.2A Continuous Output Current
- Integrated 200mΩ MOSFET
- 1.2V Reference with ±1% Accuracy
- COT Mode for Fast Load Transient
- Switching Frequency Adjustable 80KHz~1MHz
- No External VCC Capacitor is Needed
- Low Dropout Mode with DMAX>98%
- Power Good Indicator for ZCC10012
- Programmable UVLO By EN pin
- Internal Soft Start
- Cycle by Cycle High Side Peak Current Limit
- UVP with Hiccup Mode
- ULVO, TSD Protection (Non-Latch)
- SOP8 Package Available

4 Device Information

ORDER NUMBER	FUNCTION of PIN6	PACKAGE	BODY SIZE
ZCC10012SEER	PG – Power Good Indicator output	SOP8	4.9 x 3.9 x 1.45mm
ZCC10012ESEER	EXT – External bias input for IC control	SOP8	4.9 x 3.9 x 1.45mm

5 Typical Application Circuit

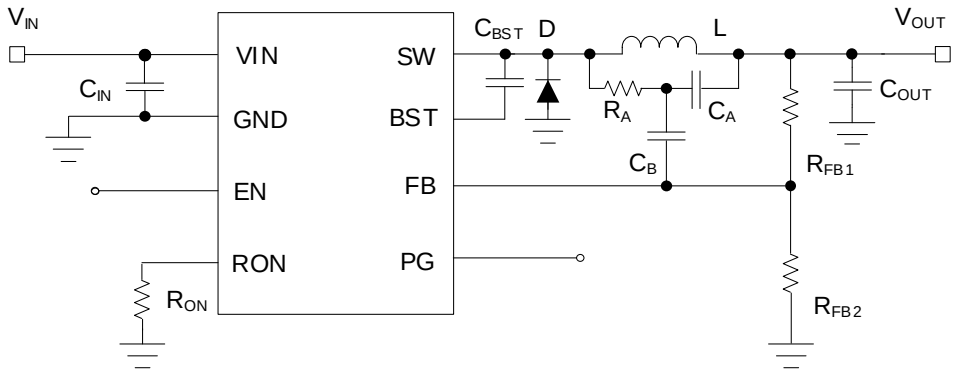


Figure 1 Typical Application Diagram of ZCC10012 with Power Good Indicator and 10μA Low Quesicent current

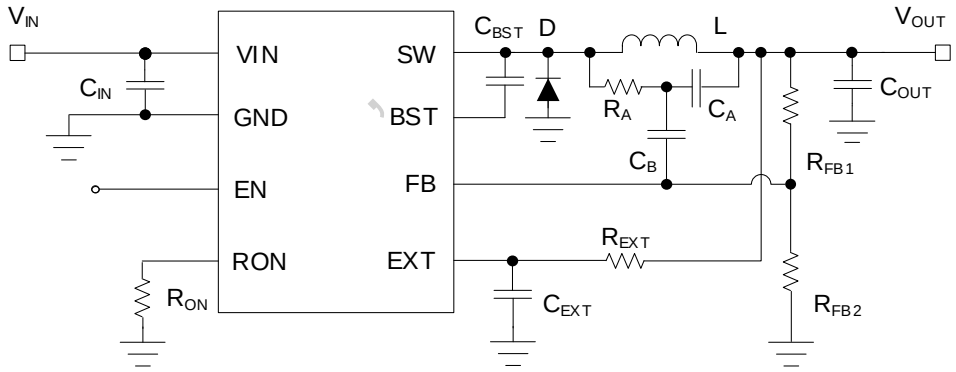
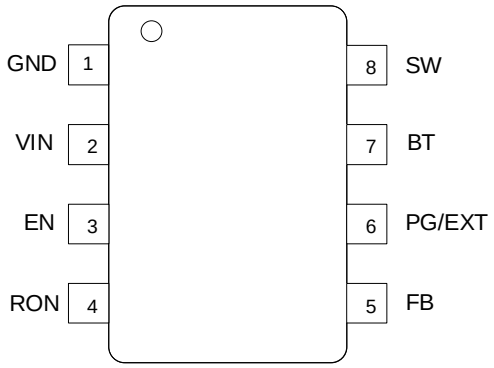


Figure 2 Typical Application Diagram of ZCC10012 with 4μA Low Quesicent current

6 Terminal Configuration and Functions

Top View



TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
1	GND	PWR	Ground pin
2	VIN	PWR	Power input node of the converter. Connect a decoupled capacitor between VIN and GND close to the IC.
3	EN	I	Enable control and input undervoltage lockout (UVLO) programming pin. Pull this pin high to turn on the device. Pull this pin to GND to disabled the device. Do not floating.
4	RON	I	Connect a resistor from this pin to GND to set the ON-time of the high-side MOS
5	FB	I	Feedback node of VOUT output voltage. Set the VOUT output voltage using the external resistor divider connected to this pin.
6	PG	I	For the ZCC10012 only: It features an open-drain power-good indicator pin. Connect to a voltage source with an external pull-up resistor.
	EXT	PWR	For ZCC10012 only: The EXT pin serves as an external power input for the SC81A10E's control circuit, designed to reduce quiescent current. The EXT pin is recommended to be connected to the VOUT of the buck or other external DC source with a voltage range of 5 - 18V. An RC filter with 10R/1μF is recommended. If not used, keep this pin floating or connect it to GND.
7	BT	PWR	Connect a 22nF X7R ceramic capacitor between BT pin and SW pin to provide the boosted bias voltage for high side gate driver.
8	SW	PWR	Switching Node. Connect to the switch node of the converter.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

PARAMETER		MIN	MAX	Unit
Voltage range at terminals(2)	VIN， EN	-0.3	105	V
	SW	-1.5	105	V
	SW less than 10ns	-5	110	V
	BT – SW	-0.3	7	V
	EXT / PG	-0.3	20	V
	FB	-0.3	6	V
T_J	Operating junction temperature range	-40	150	°C
T_{stg}	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

7.2 Handling Ratings

PARAMETER	DEFINITION		MIN	MAX	UNIT
ESD(1)	Human body model (HBM) ESD stress voltage(2)	All pins except	-1.5	1.5	kV
	Charged device model (CDM) ESD stress voltage(3)		-500	500	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

PARAMETER		MIN	TYP	MAX	UNIT
V_{IN}	VBUS voltage range	6		100	V
V_{EXT}	External power source input for the control circuit	5		18	V
V_{OUT}	VOUT voltage range	1.2			V
Icc	Continous Output Current			1.2	A
F_{SW}	Switching frequency	80		1000	kHz
C_{BT}	Bootstrap capacitor for high-side MOS driver		22		nF
T_A	Operating ambient temperature	-40		85	°C
T_J	Operating junction temperature	-40		125	°C

7.4 Thermal Information

THERMAL RESISTANCE (1)		SOP-8	UNIT
Θ_{JA}	Junction to ambient thermal resistance	94	°C/W
Θ_{JC}	Junction to case resistance	60	°C/W

(1) Measured on JESD51-7, 4-layer PCB.

7.5 Electrical Characteristics

T_J= -40~125°C and V_{IN} = 48V, V_{OUT} = 12V unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V_{IN}	Input voltage range		6		100	V
V_{IN_UVLO}	Input under voltage lock-out	Rising threshold		5.8		V
		Hysteresis		300		mV
V_{EXT}	EXT voltage range (ZCC10012)		5		18	V
V_{EXT_UV}	EXT undervoltage threshold (ZCC10012)	Rising threshold		4.65		V
		Hysteresis		200		mV
I_Q	Quiescent current into VIN	ZCC10012 or ZCC10012 with EXT disabled		8		μA
		ZCC10012 with EXT= 5~18V		3		μA
I_{SD}	Shutdown current	V_{EN}=0V,V_{IN}=48V		2		μA
POWER SWITCH						
R_{DSON_HS}	High side MOS on resistance			200		mΩ
SW_{LKG}	VEN=0V,				1	uA
FEEDBACK VOLTAGE AND SOFT START						
V_{REF}	Feedback regulation voltage	T_J = 25°C	1.188	1.2	1.212	V
		T_J = -40°C to 125°C		1.2		V
V_{FB_UV}	FB under voltage threshold			60		%V_{REF}
T_{SS}				3.6		ms
ONTIMER AND MINIMUM OFF TIMER						
T_{ON}	On-timer	VIN=48V, RON=75KΩ		650		ns
		VIN=100V, RON=75KΩ		330		ns
		VIN=48V, RON=25KΩ		240		ns
T_{MIN_ON}	Minimum on time			140		ns
T_{MIN_OFF}	Minimum off time			300		ns
T_{MAX_ON}	Maximum on time			24		us
POWER GOOD (ZCC10012)						
$V_{PG_F(FAULT)}$	PG for falling threshold (Fault)	ZCC10012 only		90		%V_{REF}
$V_{PG_R(GOOD)}$	PG for rising threshold (Good)	ZCC10012 only		95		%V_{REF}
R_{PG}	Power Good pulldown resistance	ZCC10012 only, VPG=3.3V		47		Ω
EN						
V_{EN_R}	Enable rising threshold		1.45	1.5	1.55	V
V_{EN_HYS}	Enable hysteresis			100		mV
CURRENT LIMIT						
I_{PEAK}	High-side peak current limit			2		A

THERMAL SHUTDOWN				
T_{SD}	Thermal shutdown temperature		155	°C
	Thermal shutdown hysteresis		20	°C

8 Functional Block Diagram

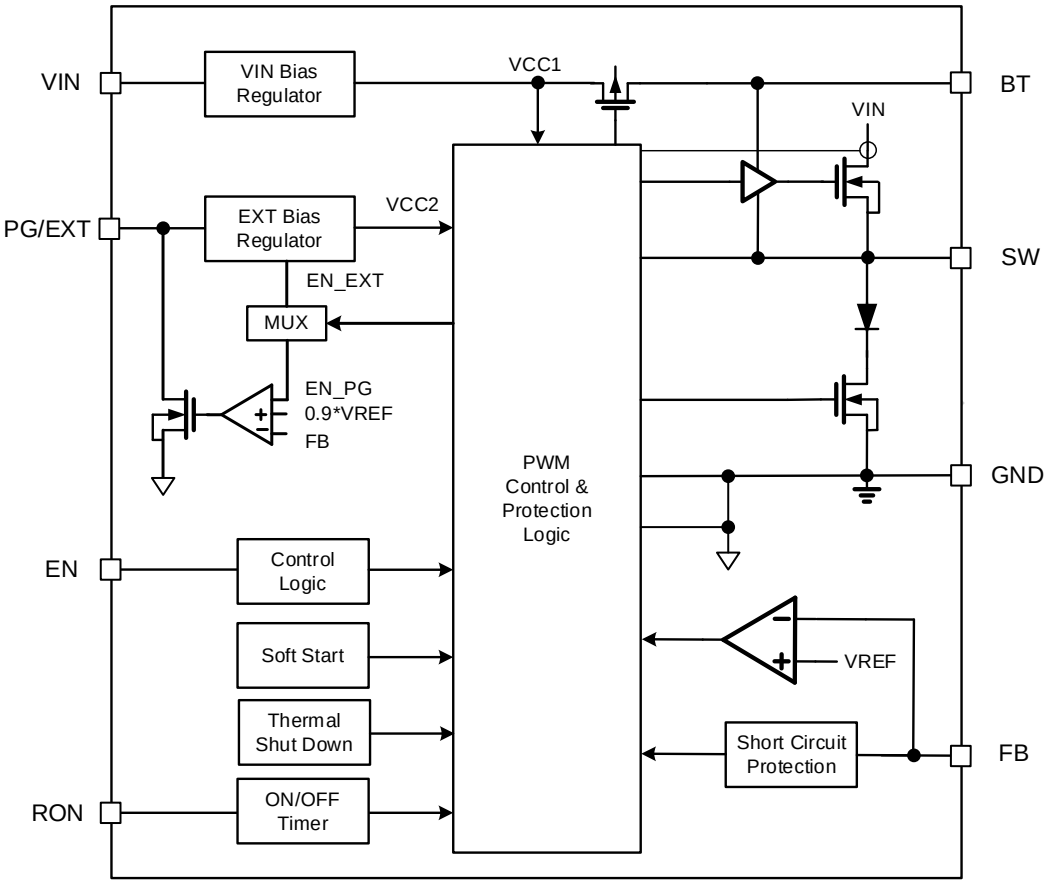


Figure.3 Functional Block Diagram

9 Feature Description

The ZCC10012 is an ultra-low quiescent current, non-synchronous buck converter. It features a wide input voltage range from 6 V to 100 V and can support up to 1.2 A continuous load current.

9.1 COT Control

The device adopts a constant on-time control mode, in which the on-period is set to be proportional to the converter input voltage. At the start of each cycle, the high-side MOSFET (HS-FET) is turned on when the feedback (FB) voltage drops below the reference voltage VREF. Subsequently, the HS-FET is turned off after the on-period expires. The HS-FET will turn on again when the FB voltage falls below VREF. This configuration ensures a pseudo-fixed frequency across the input voltage range under continuous conduction mode (CCM).

9.2 On timer

The COT ontimer is determined by the R_{ON} resistor and is inversely proportional to the input voltage V_{IN}. The R_{ON} is configured by connecting an external resistor between the RON pin and GND. The minimum on-time is limited to 120ns

The constant on-time can be calculated as:

$$t_{ON}(\mu s) = \frac{R_{ON}\ (k\Omega)}{2.5 \times V_{IN}(V)}$$

9.3 Low Dropout Operation

The device switches to a low dropout mode when it operates with a small voltages difference between the input and output. When the MOSFET is on, the on-period determined by the RON and VIN is terminated. If the FB voltage is still below the VREF, the on-period extends until the FB is equal to the VREF. Thus, the on-period is extended, and the switching frequency is reduced. The maximum on-time is limited to 24 µs, and the minimum off-time is limited to 300ns. Based on this theory, the duty cycle during the low dropout mode can approach 99%.

9.4 Enable and Disable

The device has an enable control pin EN. It is enabled when VIN rises above UVLO threshold and the EN pin voltage exceeds enable threshold of 1.2V. If the device is enabled, the converter starts switching and regulates the output voltage to the target.

9.5 Internal VCC Regulator

The IC implements an internal VCC regulator that is powered from VIN. It does not require an external capacitor to stabilize the linear regulator. The internal regulator powers the internal blocks, such as the MOSFET driver and logic circuits. The bootstrap capacitor, which is connected between the BT pin and the SW pin, is also charged through the internal VCC regulator when the SW voltage is low enough. A typical capacitance of 22nF X7R ceramic bootstrap capacitor with a voltage rating higher than 10V is recommended.

9.6 Soft Start

The IC implements a soft start feature to prevent inrush current during startup. After the IC is enabled, it ramps up the internal reference voltage in around 3.6ms. The output voltage follows the reference, so it starts up slowly.

9.7 Power Good

The ZCC10012 features an open-drain power good (PG) output to indicate whether the output voltage operates within appropriate levels. The PG signal is set to a high-impedance state when the output voltage reaches 95% of its nominal value and remains in that state until the output voltage falls below 90% of the nominal value. Note that when VIN is in UVLO or EN is pulled low, the IC shuts down and the PG signal becomes invalid. The output delay of the PG comparator is approximately 10µs to prevent false triggering.

9.8 External Power Bias Setting

The ZCC10012 features an external bias pin for further decreasing quiescent current to enhance light-load efficiency. The EXT pin is recommended to be connected to the VOUT of the buck or other external DC source with a voltage range of 5-18V. The EXT has under-voltage protection. When the EXT pin voltage is below 4.65V, the EXT bias is disabled. The internal circuit switches to VIN as the bias power. When the EXT pin voltage recovers, the bias power switches back to EXT.

9.9 Protections

9.9.1 Input Under Voltage Lock Out

The device features an input under-voltage lockout (UVLO) function to stop the operation of the converter when the input voltage drops below the typical UVLO falling threshold of 5.4V. The IC resumes normal operation when the VIN exceeds the UVLO rising threshold.

9.9.2 Peak Current Limitation

The deivce supports cycle-by-cycle peak current limit and prevents the device from high currents such as overload, output short circuit, or inductor saturation. If the peak current limit occurs, the MOSFET turns off to prevent the inductor current from running away. When the peak current is triggered, an off-timer extends the off cycle of the converter, preventing the inductor current from running away.

To prevent this function from being falsely triggered by switching noise, a minimum on-time of 120ns is adopted. However, due to this feature, the actual inductor current may exceed current limit threshold.

9.9.3 Output Short Circuit Protection

The device integrates a hiccup mode that is triggered once the voltage of the FB pin drops below 0.72V. In hiccup mode, the device periodically stops switching for 18ms and then attempts to restart with a soft start. If the short-circuit condition still persists after the soft-start cycle, the device will stop switching again. This protection mode is particularly useful when the output is continuously shorted to the ground. The average short-circuit current is significantly reduced to alleviate the thermal problem and protect the converter. Once the short-circuit condition is removed, the ZCC10012 exits the hiccup mode and returns to normal operation.

9.9.4 Over Temperature Protection

Once the IC detects that the chip junction temperature exceeds the threshold of 155 °C, the IC goes into thermal shutdown and stops switching. When the junction temperature falls below the typical value of 135°C, the IC resumes operation.

10 Application Information

10.1 Enable and Programmable UVLO

For an application enabled by VIN, if the required input under-voltage lockout (UVLO) level still follows VIN (VIN_UVLO), connect the EN pin directly to VIN. If a higher input UVLO level is needed, connect the center tap of the divider resistors between VIN and GND. This configuration sets a new under-voltage threshold and restart voltage.

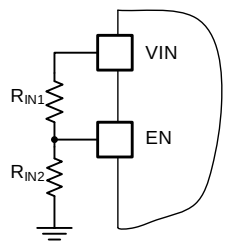


Figure.6 UVLO Threshold Programming

The new UVLO falling threshold can be calculated using the following equation.

$$V_{IN_LOW} = 1.4\text{V} \times \left(1 + \frac{\text{R}_{\text{IN1}}}{\text{R}_{\text{IN2}}}\right)$$

When the input voltage is higher than the startup threshold, the device goes back to normal operation.

$$\text{V}_{IN_HIGH} = 1.5\text{V} \times \left(1 + \frac{\text{R}_{\text{IN1}}}{\text{R}_{\text{IN2}}}\right)$$

10.2 Output Voltage Setting

The output voltage can be configured for customized values by using external feedback resistors and can be calculated as below.

$$\text{V}_{\text{OUT}} = 1.2 \text{ x } (1 + \frac{\text{R}_{\text{UP}}}{\text{R}_{\text{DOWN}}})$$

Where:

R_{UP} and R_{DOWN} are the resistors connected from VOUT to FB and AGND. Use 1% tolerance or better resistors and keep the feedback resistors close to the FB pin.

The available R_{UP} is in the range of 100KΩ to 1MΩ. A larger R_{UP} reduces standby loss but may be susceptible to noise. When considering both standby loss and noise immunity, it is recommended to select a 300~500 kΩ resistor for R_{UP}.

10.3 Switching Frequency Setting

The switching frequency of the device can be set from 80kHz to 1000kHz by connecting an external resistor between the RON pin and GND.

The switching frequency is estimated by the following equations.

$$f_{SW}(kHz) = \frac{2500 \times V_{OUT}\ (V)}{R_{ON}(k\Omega)}$$

The minimum-on-time(T_{ON_MIN}) is limited to 140ns. If the required on-time is smaller than the T_{ON_MIN}, the on-timer will be limited to T_{ON_MIN} ,which means the switching cycle is extended. In this case, the switching frequency decreses more as the duty cycle decrease. The switching frequency is roughly limited as follows:

$$f_{SW}(kHz) < \frac{V_{OUT}}{0.00014 * V_{IN_MAX}}$$

Set a proper value for the R_{ON} to ensure expected operation.

10.4 Inductor Selection

The inductor selection is a tradeoff between size, cost, efficiency, and transient response performance. The critical parameters of an inductor are inductance, DC resistance, and saturation current.

Generally, choose the inductor current ripple ΔI_L to be approximately 30% to 50% of the maximum load current. The ΔI_L selection should ensure that the peak inductor current I_{PEAK} does not exceed the current limit during the maximum output current and the maximum input voltage.

The switching frequency, input voltage, output voltage, and output ripple determine the inductor value:

$$\text{L} = \frac{V_{OUT}}{\Delta I_L \times f_{SW}} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

$$I_{PEAK} = 0.5\Delta I_L + I_{OUT_MAX}$$

The inductor saturation current should be higher than the inductor peak current.

10.5 Schottky Diode Selection

The device requires an external catch diode between the SW pin and GND. A Schottky diode with low forward voltage is preferred. The reverse breakdown voltage rating must higher than the maximum input voltage.The power rating must be greater than the peak current limit. A incompatible catch diode with not enough power rating may cause over specification voltage spike during the high side FET turns off, that may damage the device. An incompatible catch diode with an insufficient power rating may cause an over-specified voltage spike when the high-side FET is turns off, which may damage the device. It is recommended to select a Schottky diode with a higher DC current rating than the typical peak current limit of the buck converter. For example,

for ZCC10012, the typical peak current limit is 2A, select a 2A~3A Schottky diode to aqchieve enough power rating.

Check the voltage spike of the SW node during output short-circuit and the peak temperature of any components related to the power converter.

10.6 Input Capacitor Selection

The input current of the buck converter is discontinuous, and the input capacitor should be carefully selected. The device requires input decoupling capacitors and sufficient bulk capacitors. Reserve at least 4.4μF MLCCs to reduce the voltage spikes.The input voltage ripple caused by the capacitance can be calculated by:

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) + I_{OUT} \times R_{ESR}$$

Placing a electrolytic capacitor at the input can effectively suppress surges (hot-plugging) and reduce the input ripple.

10.7 Output Capacitor Selection

Since ceramic capacitors have low ESR and good high-frequency filtering, they are recommended for the best ripple performance across temperature and input voltage variations. The output voltage ripple is estimated as the following equation:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \times (1 - \frac{V_{OUT}}{V_{IN}})$$

Based on the voltage coefficient of ceramic, it loses its most capacitance at the rated voltage, so leave margin on voltage rating to ensure adequate, effective capacitance. Larger capacitors cause lower output voltage ripple and higher load transient performance.

10.8 Ripple Generation Configuration

To maintain stability, the feedback comparator requires a minimal ripple voltage of 12mV in in-phase with the inductor current during the off time. For wide VIN applications, a 20 mV ripple can be insufficient to achieve a 12 mV ripple voltage at the minimum input voltage.

10.8.1 Ripple Generator-Type 1

Type 1 ripple generation adopts a resistor (R_{ESR}) in series with the output capacitor. This ripple generation method uses the direct output voltage ripple at the lowest cost, especially for output capacitors with hundreds of milliohms of equivalent series resistance, such as aluminum electrolytic capacitors. In this way, the R_{ESR} resistor cost is also saved.

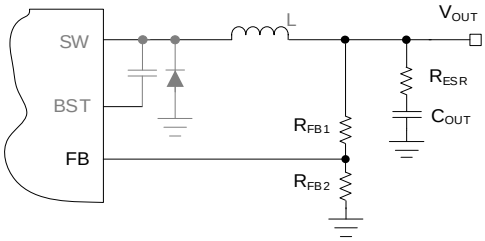


Figure.3 Type 1 Ripple Generated by R_{ESR}

The following formulas define the minimum R_{ESR} that ensures a 20mV resistive ripple component is present at the feedback node and that the generated ripple on the feedback node is in phase with the inductor current.

$$R_{ESR} \geq \frac{20mV * V_{OUT}}{V_{FB} * \Delta I_L}$$

$$R_{ESR} \geq \frac{V_O}{2 * V_{IN} * F_{SW} * C_{OUT}}$$

10.8.2 Ripple Generator-Type 2

Type 2 ripple generator adopts a C_{FF} capacitor in addition to the R_{ESR} resistor. It can tolerate a lower R_{ESR} value compared to the Type 1 ripple generator, enabling it to deliver a lower output voltage ripple.

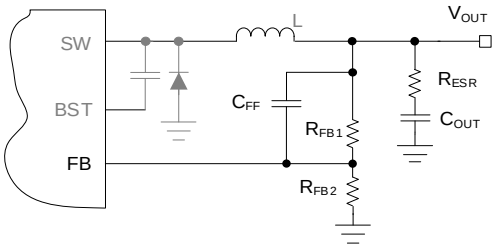


Figure.4 Type 2 Ripple Generated by R_{ESR}& C_{FF}

Similar to the type 1 generator, the R_{ESR} can be calculated using the following formulas:

$$R_{ESR} \geq \frac{20mV}{\Delta I_L}$$

$$R_{ESR} \geq \frac{V_O}{2 * V_{IN} * F_{SW} * C_{OUT}}$$

The minimum feed-forward capacitance, CFF:

$$C_{FF} \geq \frac{10}{2\pi * \mathrm{F_{SW}} * (\mathrm{R_{FB1}} // \mathrm{R_{FB2}})}$$

10.8.3 Ripple Generator-Type 3

Type 3 ripple generator adopts an RC filter composed of R_A and C_A, and uses the switch voltage to generate a triangular ramp that is in phase with the inductor current. This ripple generator does not need output ripple any more. It supports utra-low ESR output capacitors, such as ceramic capacitors.

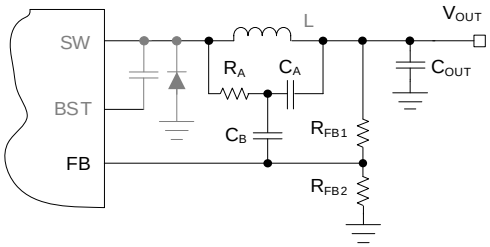


Figure.5 Type 3 Ripple Generated by RCC

The $R_A C_A$ filter provides the required amplitude and phase of the ripple at the feedback node. keep R_A within practical limits between 100 kΩ and 1 MΩ. A smaller R_A may need to be used to operate with an input voltage below 48V. Design the FB ripple to be 12mV or more at the minimum input voltage to ensure stability.

$$C_A \geq \frac{10}{F_{SW} * (R_{FB1} // R_{FB2})}$$

$$R_A C_A \leq \frac{(V_{IN} - V_{OUT}) * T_{ON}}{20mV}$$

The coupling capacitance C_B based on the load transient response settling time, T_{TRS}:

$$C_B \geq \frac{T_{TRS}}{3 * R_{FB1}}$$

10.9 Power Good

For ZCC10012, the power good indicator PG pin is an open-drain power good (PG) output. An external pull-up resistor with a typical resistance ranging from 10kΩ to 100kΩ is required to connect the PG pin to an external voltage of less than 20V.

The PG pin can be left floating if unused.

10.10 External Power Bias Setting

For ZCC10012, to further decrease quiescent current for enhance light-load efficiency, the EXT pin is recommended to be connected to the VOUT of the buck or other external DC source with a voltage range of 5-18V. A 10Ω/1μF RC filter is recommended to be placed close to the IC to suppress voltage transients during supply changes. If not used, keep this pin floating or connect it to GND.

11 Layout Guide

For a COT buck converter, the layout design is a critical step. Improper layout design may lead to converter instability, noise issues, thermal problems, etc. A reasonable PCB design is the key to the safe, efficient and stable operation of the IC. The following are some PCB design rules for your reference:

1) Place the inductor and Schottky diode close to the SW pin. Minimize the area of the SW trace or plane to prevent excessive capacitive coupling. The input MLCCs (CVIN) should be placed as close as possible to the VIN and the Schottky diode to minimize the buck hot loop.

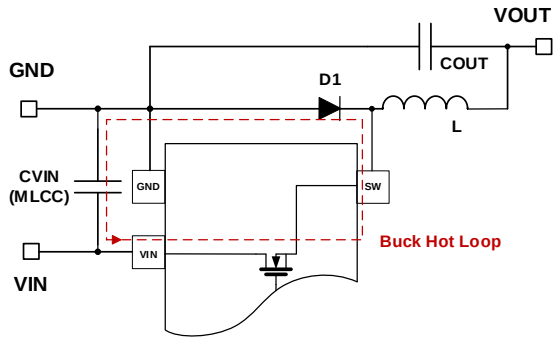


Figure.6 Minimizing the Hot Loop Helps Mitigate EMI

2) A large-area copper pour should be created to connect the GND pins of the IC and those of the input MLCCs. Additionally, some metallized vias should be placed to connect the top copper area to the internal GND layers. This approach can minimize the GND impedance and maximize the thermal performance.

3) The dividing resistors for the output feedback should be placed close to the FB pin and kept away from the SW node and indctor. Ensure that the FB trace is as short as possible.

4) The BT capacitor should be placed as close as possible to the BT/SW pins of the IC, ensuring that the traces are as short as possible.

5) Place the RON resistor as close as possible to the device and route the trace with minimal length. The parasitic capacitance from RON to GND must not exceed 20 pF.

6) For ZCC10012, place the RC filter of EXT as close as possible to the device and route the trace with minimal length.

The following figures provide a typical reference for PCB design.

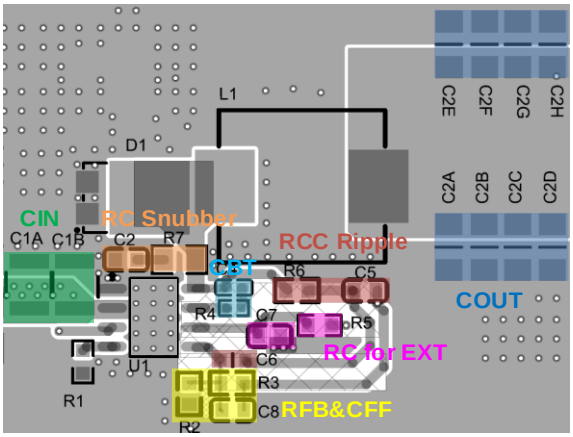
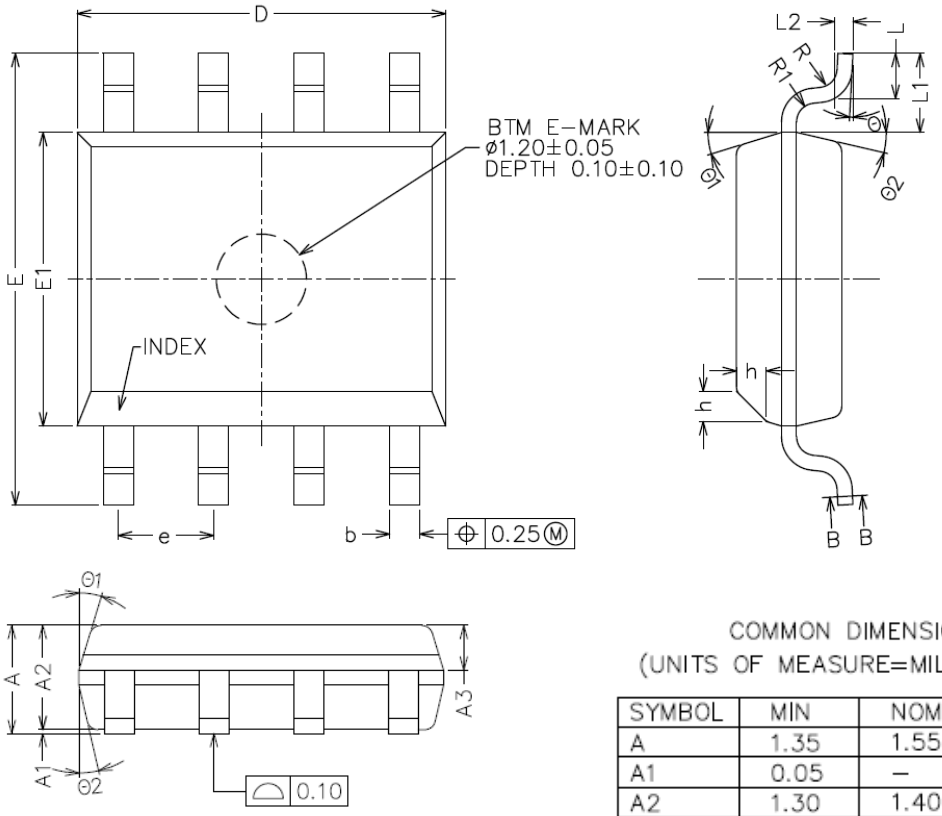


Figure.7 PCB layout Example

MECHANICAL DATA

SOP8



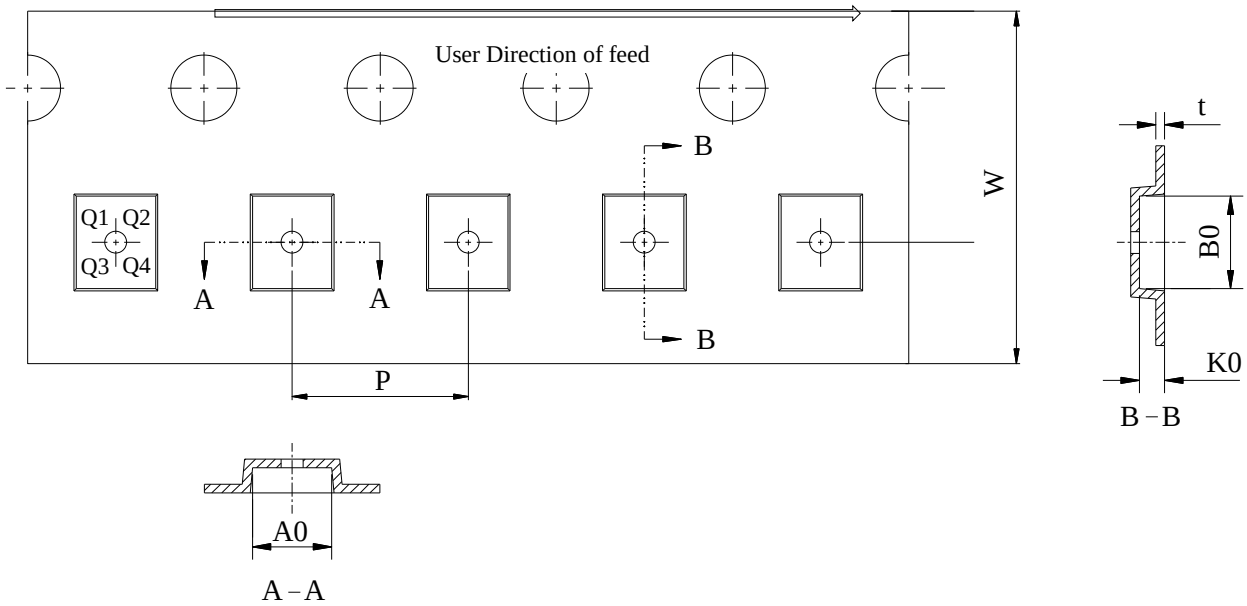
COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.05	–	0.25
A2	1.30	1.40	1.50
A3	0.50	0.60	0.70
b	0.38	–	0.47
b1	0.37	0.40	0.43
c	0.17	–	0.25
c1	0.17	0.20	0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.17	1.27	1.37
L	0.45	0.60	0.80
L1	1.04REF		
L2	0.25BSC		
R	0.07	–	–
R1	0.07	–	–
h	0.30	0.40	0.50
Θ	0°	–	8°
Θ1	15°	17°	19°
Θ2	11°	13°	15°

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MS-012 AA
DO NOT INCLUDE MOLD FLASH OR PROTRUSION.

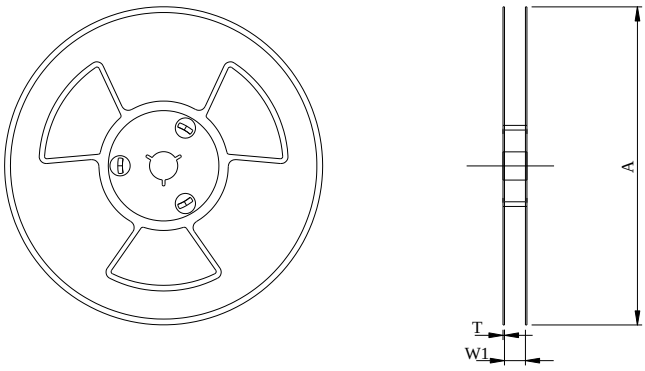
TAPE AND REEL INFORMATION

Carrier Tape



Item	W	P	A0	B0	K0	t	Pin1 Quadrant
Size (mm)	12±0.3	8±0.1	6.55±0.15	5.3±0.1	2±0.15	0.25±0.05	Q1

REEL



Item	A	W1	T
Size (mm)	330±2	12.4^{+2}_{-0}	1.5±0.3