ZCC33xx 3.9-µA, SC70-3, SOT-23-3, and UQFN-8, 30-ppm/°C Drift Voltage Reference

1 Features

- Microsize Packages: SC70-3, SOT-23-3, UQFN-8
- Low Supply Current: 3.9 µA (typ)
- Extremely Low Dropout Voltage: 110 mV (typ)
- High Output Current: ±5 mA
- Low Temperature Drift: 30 ppm/°C (max)
- High Initial Accuracy: ±0.15% (max)
- 0.1-Hz to 10-Hz Noise: 35 μV_{PP} (ZCC3312)
- Voltage Options: 1.2 V, 1.8 V, 2.5 V, 3 V, 3.3 V

2 Applications

- Portable Equipment
- Tablets and Smartphones
- Hard Disk Drives
- Sensor Modules
- Data Acquisition Systems
- Medical Equipment
- Test Equipment

3 Description

The ZCC33xx is a low-power, precision, low-dropout voltage reference family available in tiny SC70-3 and SOT-23-3 packages, and in a 1.5-mm × 1.5-mm UQFN-8 package. Small size and low power consumption (5-µA max) make the ZCC33xx ideal for a wide variety of portable and battery-powered applications.

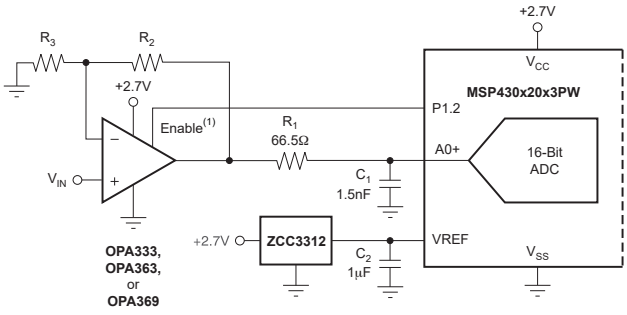
The ZCC33xx can be operated at a supply voltage 180 mV above the specified output voltage under normal load conditions, with the exception of the ZCC3312, which has a minimum supply voltage of 1.7 V. All models are specified for the wide temperature range of –40°C to +125°C.

Device Information(1)

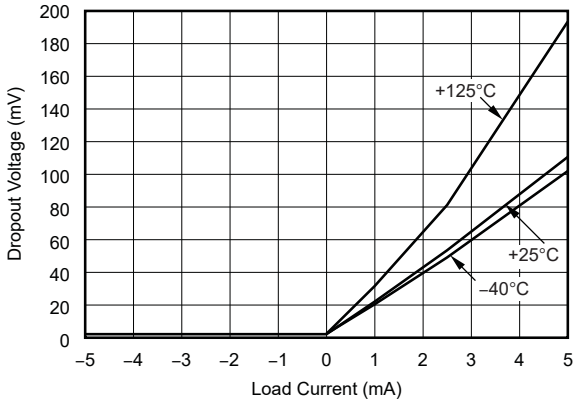
PART NUMBER	PACKAGE	BODY SIZE (NOM)
ZCC33xx	SOT-23 (3)	2.92 mm × 1.30 mm
	SC70 (3)	2.00 mm × 1.25 mm
	UQFN (8)	1.50 mm × 1.50 mm

(1) For all available packages, see the package option addendum at the end of the datasheet.

ZCC3312 in a Single-Supply Signal Chain



Dropout Voltage vs Load Current



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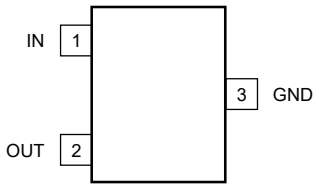
4 Device Comparison

PRODUCT	DESCRIPTION
ZCC3312	1.25 V
ZCC3318	1.8 V
ZCC3320	2.048 V
ZCC3325	2.5 V
ZCC3330	3.0 V
ZCC3333	3.3 V

5 Pin Configuration and Functions

ZCC3312, ZCC3318, ZCC3320, ZCC3325, ZCC3330, ZCC3333 DBZ Package and DCK Package SOT-23-3, SC70-3 (Top View)



ZCC3312, ZCC3318, ZCC3320, ZCC3325, ZCC3330, ZCC3333 RSE Package UQFN-8 (Top View)

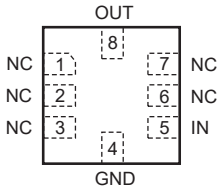


Table 1. Pin Functions

PIN			DESCRIPTION
NAME	DBZ, DCK	RSE	
GND	3	4	Ground
IN	1	5	Input supply voltage
NC	—	1, 2, 3, 6, 7	Not connected
OUT	2	8	Output voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted).[1]

		MIN	MAX	UNIT
Voltage	Input voltage		7.5	V
	Output voltage		5	
Current	Output short-circuit, I_{SC}[2]		180	mA
Temperature	Operating	–50	150	°C
	Junction, T_J		150	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) See the *Power-Supply Recommendations* section of this data sheet.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±4000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	
	Machine model (MM)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted).

		MIN	NOM	MAX	UNIT
V_{IN}	Supply input voltage[1]	V_{OUT} + 0.2		5.5	V
I_{OUT}	Output current range	–5		5	mA

(1) The minimum supply voltage for the ZCC3312 is 1.7 V.

6.4 Thermal Information

THERMAL METRIC[1]		ZCC33xx		ZCC3325, ZCC3330	UNIT
		DCK (SC70)	DBZ (SOT-23)	RSE (UQFN)	
		3 PINS	3 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	279.7	313.1	61.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	136.3	144.0	32.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.9	109.3	16.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.0	18.2	1.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	56.1	107.9	16.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

At T_A = 25°C, V_{IN} = 5 V, and I_{LOAD} = 0 mA (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ZCC3312 (1.25 V)						
V_{OUT}	Output voltage			1.25		V
	Initial accuracy		–0.15%		0.15%	
	Output voltage noise	f = 0.1 Hz to 10 Hz		35		μV_{PP}
ZCC3318 (1.8 V)						
V_{OUT}	Output voltage			1.8		V
	Initial accuracy		–0.15%		0.15%	
	Output voltage noise	f = 0.1 Hz to 10 Hz		50		μV_{PP}
ZCC3320 (2.048 V)						
V_{OUT}	Output voltage			2.048		V
	Initial accuracy		–0.15%		0.15%	
	Output voltage noise	f = 0.1 Hz to 10 Hz		55		μV_{PP}
ZCC3325 (2.5 V)						
V_{OUT}	Output voltage			2.5		V
	Initial accuracy		–0.15%		0.15%	
	Output voltage noise	f = 0.1 Hz to 10 Hz		70		μV_{PP}
ZCC3330 (3.0 V)						
V_{OUT}	Output voltage			3.0		V
	Initial accuracy		–0.15%		0.15%	
	Output voltage noise	f = 0.1 Hz to 10 Hz		84		μV_{PP}
ZCC3333 (3.3 V)						
V_{OUT}	Output voltage			3.3		V
	Initial accuracy		–0.15%		0.15%	
	Output voltage noise	f = 0.1 Hz to 10 Hz		92		μV_{PP}
ZCC33xx (ZCC3312, ZCC3320, ZCC3325, ZCC3330, ZCC3333, ZCC3340)						
dV_{OUT}/dT	Output voltage temperature drift	–40°C to 85°C		9	30	ppm/°C
		–40°C to 125°C		8	30	
$\Delta V_{O(\Delta VI)}$	Line regulation	V_{IN} = V_{OUT} + 200 mV to 5.5 V(1)	–50	6	50	ppm/V
		0°C to +70°C		6		
		–40°C to 85°C		8		
		–40°C to 125°C		30		
$\Delta V_{O(\Delta IL)}$	Load regulation	V_{IN} = V_{OUT} + 200 mV(1)	–50	6	50	ppm/mA
		I_{LOAD} = ±5 mA, 0°C to 70°C		10		
		–40°C to 85°C		20		
		–40°C to 125°C		20		
	Long-term stability(2)	0h to 1000h at 25°C		55		ppm
dT	Thermal hysteresis(3)			90		ppm
$V_{IN} – V_{OUT}$	Minimum dropout voltage(1)	I_{LOAD} = ±5 mA		110	160	mV
		0°C to 70°C		120		
		–40°C to 85°C		135		
		–40°C to 125°C		180		
		I_{LOAD} = ±2 mA, –40°C to 85°C			70	
I_{SC}	Short-circuit current	Sourcing and sinking		35		mA
	Capacitive load		0.1		10	µF
	Turn-on settling time	To 0.1% with C_L = 1 µF		2		ms

(1) The minimum supply voltage for the ZCC3312 is 1.7 V.
(2) The long-term stability number reduces as the time increases.
(3) The thermal hysteresis procedure is explained in more detail in the *Thermal Hysteresis* section.

Electrical Characteristics (continued)

At T_A = 25°C, V_{IN} = 5 V, and I_{LOAD} = 0 mA (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_S	Specified voltage range		V_{OUT} + 0.2[1]		5.5	V
	Operating voltage range	I_{LOAD} = 0 mA		V_{OUT} + 0.005	5.5	V
I_Q	Current			3.9	5	μA
		–40°C to 85°C		4.4	6.5	
		–40°C to 125°C		4.8	8.5	
TEMPERATURE						
T_A	Specified range		–40		125	°C
	Operating range		–50		150	

6.6 Typical Characteristics

At T_A = 25°C and V_{IN} = 5 V, and ZCC3325 used for typical characteristic measurements (unless otherwise noted).

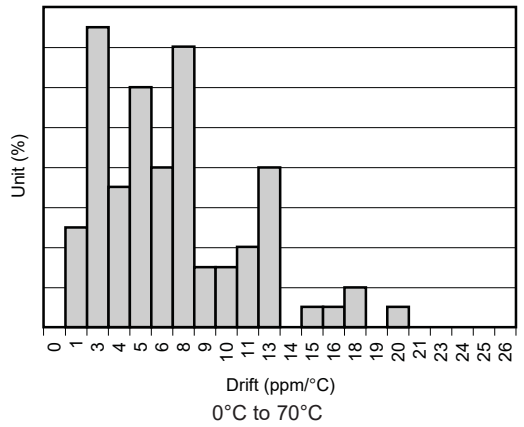


Figure 1. Temperature Drift

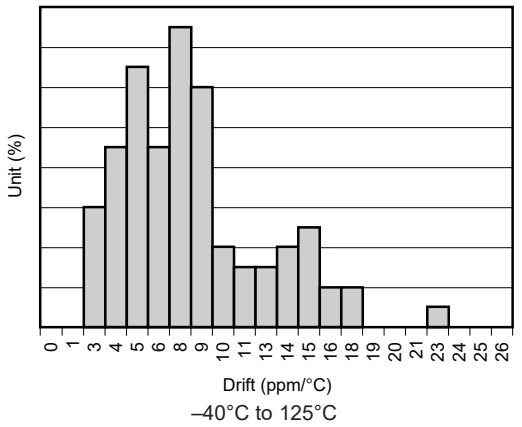


Figure 2. Temperature Drift

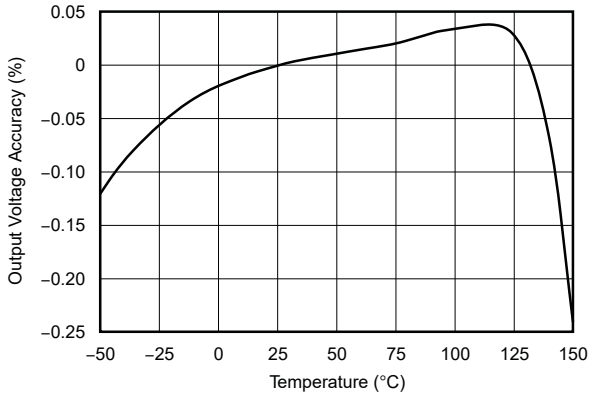


Figure 3. Output Voltage Accuracy vs Temperature

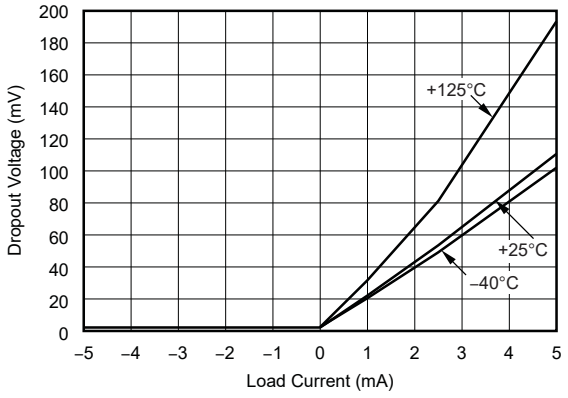


Figure 4. Dropout Voltage vs Load Current

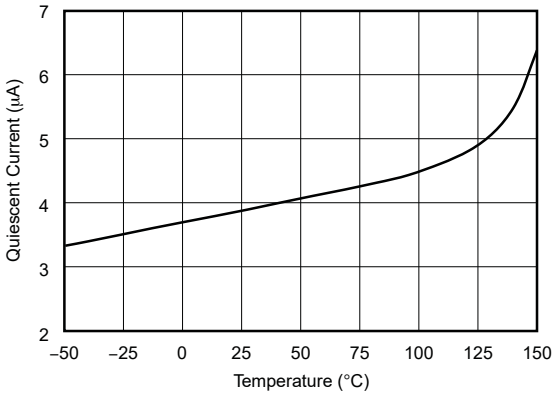


Figure 5. Quiescent Current vs Temperature

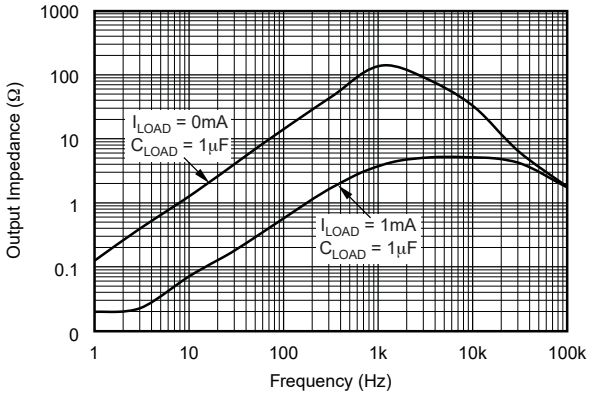


Figure 6. Output Impedance vs Frequency

Typical Characteristics (continued)

At T_A = 25°C and V_{IN} = 5 V, and ZCC3325 used for typical characteristic measurements (unless otherwise noted).

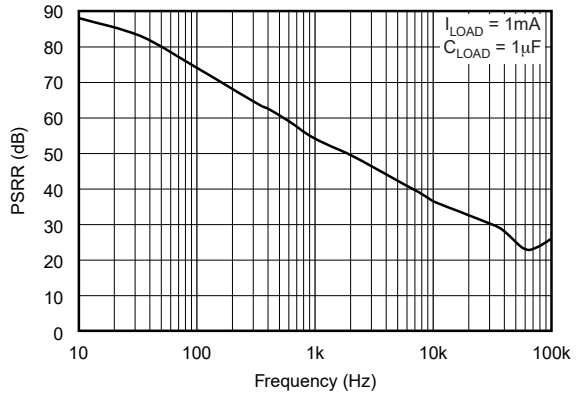


Figure 7. Power-Supply Rejection Ratio vs Frequency

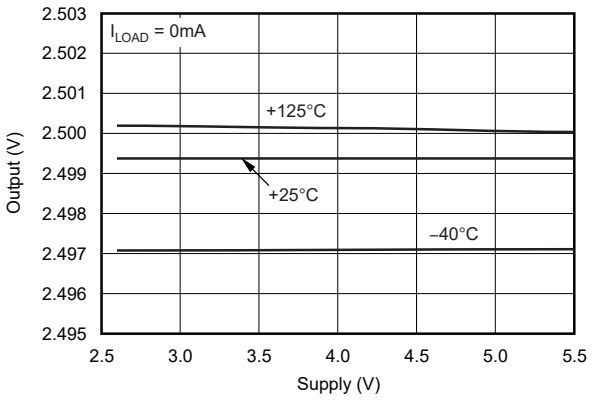


Figure 8. Output vs Supply

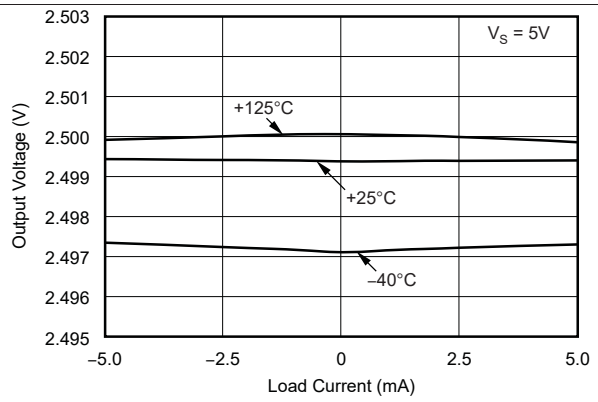


Figure 9. Output Voltage vs Load Current

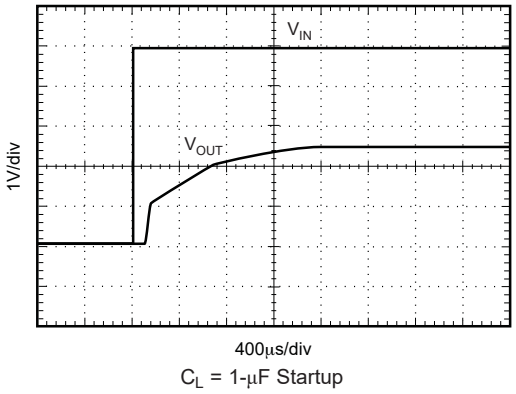


Figure 10. Step Response

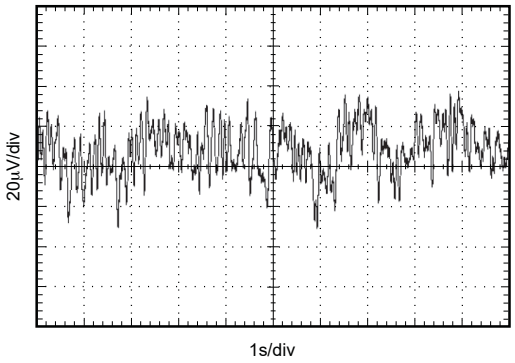


Figure 11. 0.1-Hz to 10-Hz Noise

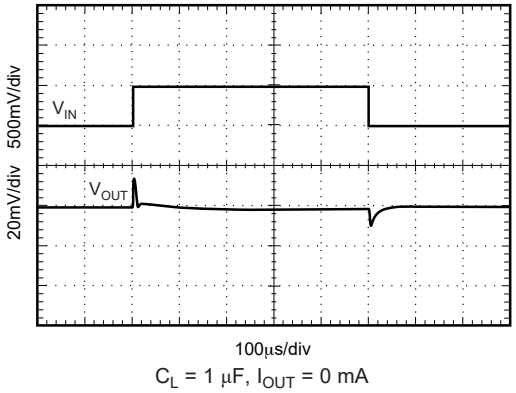
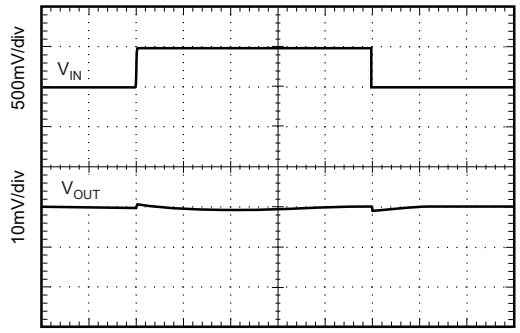


Figure 12. Line Transient

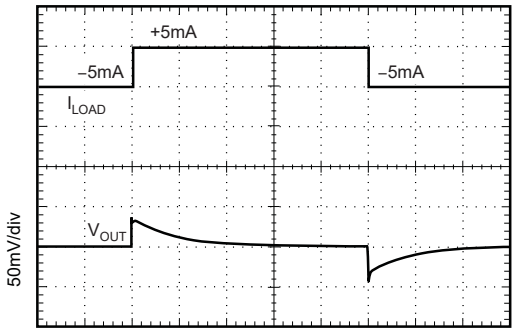
Typical Characteristics (continued)

At T_A = 25°C and V_{IN} = 5 V, and ZCC3325 used for typical characteristic measurements (unless otherwise noted).



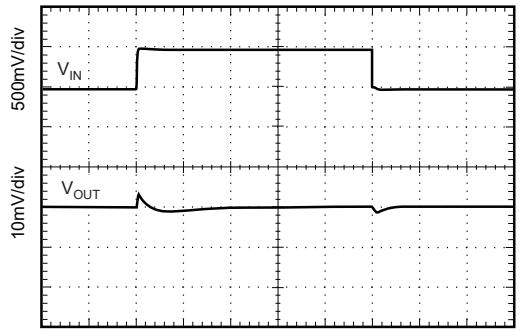
C_{LOAD} = 10 µF, I_{OUT} = 0 mA

Figure 13. Line Transient



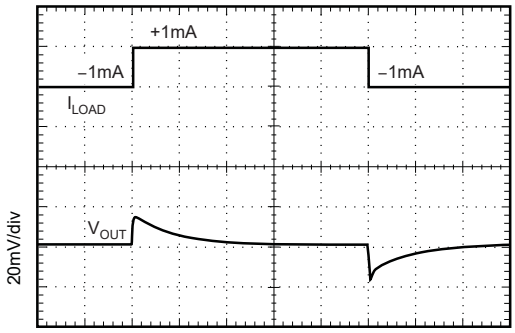
C_L = 1 µF, ±5-mA Output Pulse

Figure 14. Load Transient



C_{LOAD} = 10 µF, I_{OUT} = 1 mA

Figure 15. Line Transient



C_L = 1 µF, ±1-mA Output Pulse

Figure 16. Load Transient

7 Parameter Measurement Information

7.1 Thermal Hysteresis

Thermal hysteresis for the ZCC33xx is defined as the change in output voltage after operating the device at 25°C, cycling the device through the specified temperature range, and returning to 25°C. It can be expressed as Equation 1:

$$V_{HYST} = \left(\frac{|V_{PRE} - V_{POST}|}{V_{NOM}} \right) \cdot 10^6 \text{ (ppm)}$$

where

- V_{HYST} = thermal hysteresis (in units of ppm).
- V_{NOM} = the specified output voltage.
- V_{PRE} = output voltage measured at 25°C pretemperature cycling.
- V_{POST} = output voltage measured after the device cycles from 25°C through the specified temperature range of –40°C to 125°C and returns to 25°C. (1)

8 Detailed Description

8.1 Overview

The ZCC33xx is a family of low-power, precision band-gap voltage references that are specifically designed for extremely low dropout, excellent initial voltage accuracy with a high output current. A simplified block diagram of the ZCC33xx is shown in the *Functional Block Diagram* section. Figure 17 shows the typical connections for the ZCC33xx. A supply bypass capacitor ranging between 1 μF to 10 μF is recommended. The total capacitive load at the output must be between 0.1 μF to 10 μF to ensure output stability.

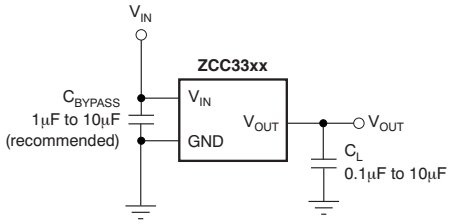
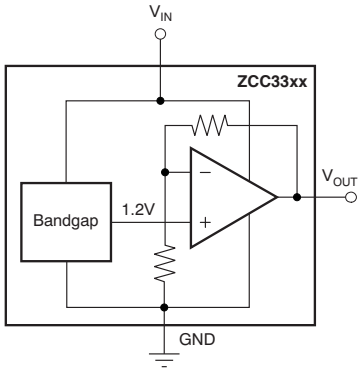


Figure 17. Basic Connections

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Start-Up Time

The ZCC33xx features an advanced start-up circuit. Start-up time is almost independent of load (with a 0.1-μF to 10-μF load). Upon startup, the current boost circuit forces the output voltage. When the preset voltage is reached, the ZCC33xx switches to the second stage of output circuitry to precisely set the output voltage. Figure 18 shows the start-up time of the ZCC3325 for three different capacitive loads. In all three cases, the output voltage settles within 2 ms.

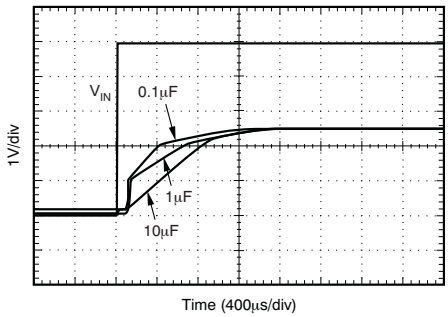


Figure 18. Start-Up Time

Feature Description (continued)

8.3.2 Low Temperature Drift

The ZCC33xx is designed for minimal drift error, defined as the change in output voltage over temperature. The drift is calculated using the box method, as described in Equation 2:

$$\text{Drift} = \left(\frac{V_{OUTMAX} - V_{OUTMIN}}{V_{OUT} \cdot \text{Temperature Range}}\right) \cdot 10^6 \text{ (ppm)} \tag{2}$$

8.3.3 Power Dissipation

The ZCC33xx family is specified to deliver current loads of ±5 mA over the specified input voltage range. The temperature of the device increases according to Equation 3:

$$T_J = T_A + P_D \cdot R_{\theta JA}$$

where

- T_J = junction temperature (°C).
- T_A = ambient temperature (°C).
- P_D = power dissipation (W) = $V_{IN} \times I_Q + (V_{IN} - V_{OUT})\, I_{OUT}$.
- $R_{\theta JA}$ = Junction-to-ambient thermal resistance (°C/W). (3)

The ZCC33xx junction temperature must not exceed the absolute maximum rating of 150°C.

8.3.4 Noise Performance

Typical 0.1-Hz to 10-Hz voltage noise for each member of the ZCC33xx family is specified in the *Electrical Characteristics* table. The noise voltage increases with output voltage and operating temperature. Use additional filtering to improve output noise levels. Give special attention to ensure that the output impedance does not degrade output voltage accuracy.

8.4 Device Functional Modes

The ZCC33xx is powered on when the voltage on the IN pin is greater than V_{OUT} + 0.2 V, except for the ZCC3312, where the minimum supply voltage is 1.7 V. The maximum input voltage for the ZCC33xx is 5.5 V. Use a supply bypass capacitor ranging between 1 μF to 10 μF. The total capacitive load at the output must be between 0.1 μF to 10 μF to ensure output stability.

9 Applications and Implementation

9.1 Application Information

The ZCC33xx is a family of low-power, precision band-gap voltage references that are specifically designed for extremely low dropout, excellent initial voltage accuracy with a high output current. The extremely small size of the SC70-3, SOT-23-3, and UQFN-8 make these references very attractive for space-constrained applications. The following section describes one common application.

9.2 Typical Applications

9.2.1 ZCC3312 in a Bipolar Signal-Chain Configuration

The circuit in Figure 19 consists of a low-power reference and conditioning circuit. This circuit attenuates and level-shifts a bipolar input voltage within the proper input range of a single-supply, low-power, 16-bit ΔΣ analog-to-digital converter (ADC), such as the one inside the MSP430 (or other similar single-supply ADCs). Precision reference circuits are used to level-shift the input signal, provide the ADC reference voltage, and create a well-regulated supply voltage for the low-power analog circuitry. A low-power, zero-drift op amp circuit is used to attenuate and level-shift the input signal.

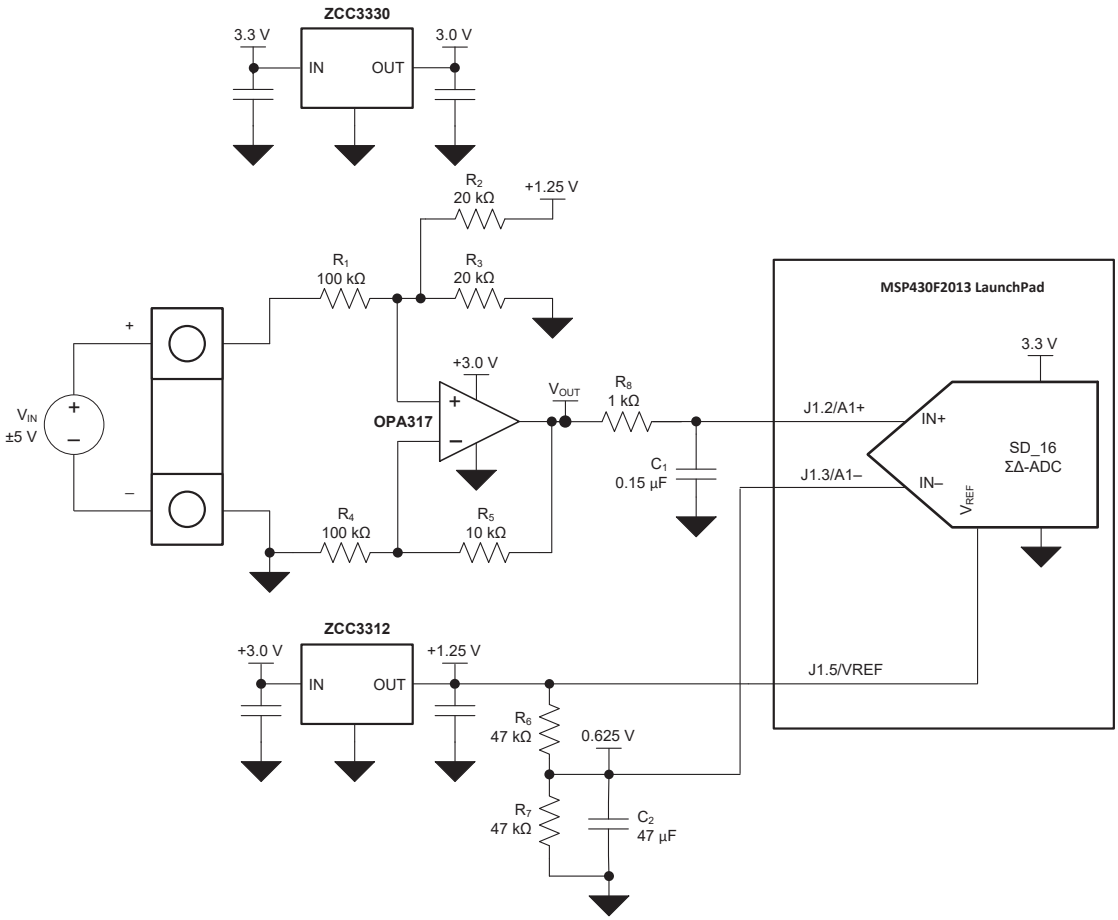


Figure 19. Bipolar Signal-Chain Configuration

Typical Applications (continued)

9.2.1.1 Design Requirements

The design requirements are as follows:

- Supply voltage: 3.3 V
- Maximum input voltage: ±6 V
- Specified input voltage: ±5 V
- ADC reference voltage: 1.25 V

9.2.1.2 Detailed Design Procedure

Figure 19 depicts a simplified schematic for this design showing the MSP430 ADC inputs and full input conditioning circuitry. The ADC is configured for a bipolar measurement where final conversion result is the differential voltage, V_{DIFF}, between the positive and negative ADC inputs, A1+ and A1–. The bipolar, ground-referenced input signal must be level-shifted and attenuated by the op amp so that the output is biased to V_{REF} / 2 and has a differential voltage that is within the $\pm V_{REF}$ / 2 input range of the ADC. The transfer function for the op-amp circuit simplifies to Equation 4.

$$A1+ = \left(\frac{R_3}{R_2 + R_3}\right)V_{REF} + \left(\frac{R_2 \parallel R_3}{R_1}\right)V_{IN}$$

where

- $R_1 = R_4$
- $R_5 = R_2 \parallel R_3$ (4)

The voltage applied to the negative ADC input, A1–, is based on the resistor divider formed by R6 and R7 and is set to V_{REF} / 2 by setting R6 equal to R7, as shown in Equation 5.

$$A1- = \left(\frac{R_7}{R_6 + R_7}\right)V_{REF} = \frac{V_{REF}}{2} \quad (5)$$

9.2.1.2.1 Op Amp Level-Shift Design

The ratio of R_2, R_3, and the V_{REF} voltage determines the voltage on the output of the op amp when the differential input is 0 V. Select the components so that V_{OUT} is equal to the V_{REF} / 2 voltage when V_{IN} is equal to 0 V, as shown in Equation 6.

$$A1+ = \frac{V_{REF}}{2} = \left(\frac{R_3}{R_2 + R_3}\right)V_{REF}$$

where

- $V_{IN} = 0$ V
- $R_2 = R_3$ (6)

Solve for the value of R_5 by setting R_3 equal to R_2 in Equation 4, as shown in Equation 7:

$$R_5 = \left(\frac{R_2 \cdot R_2}{R_2 + R_2}\right) = \frac{R_2^2}{2 \cdot R_2} = \frac{R_2}{2} \quad (7)$$

9.2.1.2.2 Differential Input Attenuator Design

V_{DIFF} is the difference between the two inputs, as shown in Equation 8:

$$V_{DIFF} = (A1+) - (A1-) = \left(\frac{R_3}{R_2 + R_3}\right)V_{REF} + \left(\frac{R_2 \parallel R_3}{R_1}\right)V_{IN} - \frac{V_{REF}}{2} \quad (8)$$

Typical Applications (continued)

When the ratio of R_3 and R_2 equals the ratio of R_7 and R_6, Equation 8 simplifies to Equation 10.

That is, if:

$$\left(\frac{R_3}{R_2 + R_3}\right)V_{REF} = \left(\frac{R_7}{R_6 + R_7}\right)V_{REF} = \frac{1}{2}V_{REF} \tag{9}$$

Then:

$$V_{DIFF} = \left(\frac{R_2 \parallel R_3}{R_1}\right)V_{IN} \tag{10}$$

Determine the ratio of R_1, R_2, and R_3 by setting A1+ equal to the maximum V_{DIFF} for a full-scale positive or negative input voltage, VIN_MAX, as shown in Equation 11:

$$A1+ = V_{DIFF_MAX} = \left(\frac{R_2 \parallel R_3}{R_1}\right)V_{IN_MAX} \tag{11}$$

R_2 equals R_3; therefore, Equation 11 simplifies to R_2 / 2, resulting in Equation 12:

$$V_{DIFF_MAX} = \left(\frac{R_2}{2 \cdot R_1}\right)V_{IN_MAX} \tag{12}$$

9.2.1.2.3 Input Filtering

Both inputs feature first-order, low-pass, antialiasing filters that limit the bandwidth and noise of the input signals applied to the ADC. The A1+ filter is formed by R_8 and C_1 and the equation for the –3-dB cutoff frequency is shown in Equation 13:

$$f_{-3dB_A1+} = \frac{1}{2 \cdot \pi \cdot R_8 \cdot C_1} \tag{13}$$

The A1– input filter is formed by C_2 and the parallel combination of the R_6 and R_7 resistors, as shown in Equation 14:

$$f_{-3dB_A1-} = \frac{1}{2 \cdot \pi \cdot \left(\frac{R_6}{2}\right) \cdot C_2} \tag{14}$$

9.2.1.2.4 Component Selection

9.2.1.2.4.1 Voltage References

The ZCC33xx series of precision low-power voltage references pair well with the low power consumption of the MSP430, while achieving the target accuracy goals. The 16-bit converter in the MSP430F2013 accepts an external reference voltage from 1 V to 1.5 V with a typical reference input of 1.25 V, as shown in Table 2.

Table 2. SD16_A, External Reference Input (MSP430F20x3)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{REF(I)}$	Input voltage range	VCC = 3 V, SD16REFON = 0	1	1.25	1.5	V
$I_{REF(I)}$	Input current	VCC = 3 V, SD16REFON = 0			50	nA

(1) Over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted).

The ZCC3312 provides the desired 1.25-V reference voltage for the MSP430 ADC. The accuracy of the ZCC3312 output, shown in the *Electrical Characteristics*, directly affects the accuracy of the entire system and must be less than the desired unadjusted error goals. The ZCC3312 maximum ±0.15% initial accuracy specification is equal to the unadjusted error design goal of 0.15%, indicating that most of the error budget in this design must be devoted to the reference accuracy.

The 3.3-V system supply voltage that powers the MSP430 can also supply other devices, and therefore may have regulation and noise issues. The ZCC3330 creates an accurate and stable 3.0 V output used by the op amp, ZCC3312, and other low-power analog circuitry. The ZCC33xx series has a drop-output voltage of V_{OUT} + 200 mV; therefore, as long as the input supply remains above 3.2 V, the ZCC3330 produces a regulated 3.0 V output. The output current for the ZCC33xx series is specified at ±5 mA, as shown in Figure 9, and is sufficient for the ZCC3312 and a low-power op amp.

9.2.1.2.4.2 Op Amp

The OPA317 op amp is used because of low offset voltage, low offset voltage drift, CMRR, and low power consumption. The dc specifications for the OPA317 can be seen in the OPA317 data sheet, SBOS682, available for download from www.ti.com. The maximum offset of 100 µV accounts for only 0.001% of the full-scale signal, and the low-drift reduces temperature drift effects. Therefore, as previously mentioned, most of the error in this design is from the reference accuracy and passive component tolerances.

9.2.1.2.5 Input Attenuation and Level Shifting

For this design, the bipolar ±5-V input must be attenuated and level shifted so the differential voltage is within the input range of $\pm V_{REF}$ / 2, or ±0.625 V. The accuracy of the op amp output and ADC input may degrade near the supply rails and V_{REF} voltage, so the output is designed to produce a 0.125 V to 1.125 V output, or ±0.5 V for a ±5 V input. Scaling the output this way also increases the allowable input range to ±6 V, and allows for some underscale and overscale voltage measurement and protection.

Use Equation 12 to scale the ±5-V input to a ±0.5-V differential voltage, as shown in Equation 15.

$$0.5\ \text{V} = \left(\frac{R_2}{2 \cdot 100\ \text{k}\Omega}\right) \cdot 5\ \text{V}$$

where

- $R_1 = R_4 = 100\ \text{k}\Omega$ (15)

R_1 and R_4 dominate the input impedance for this design and are therefore selected to be 100 kΩ. Higher values can be selected to increase the input impedance at the expense of input noise.

With the value for R_2 and R_3 selected as 20 kΩ, the value for R_5 is calculated, as shown in Equation 16:

$$R_5 = \left(\frac{R_2}{2}\right) = 10\ \text{k}\Omega$$

where

- $R_2 = R_3 = 20\ \text{k}\Omega$ (16)

In order for A1– to equal to V_{REF} / 2, R_6 must equal R_7. Two 47-kΩ resistors are used in order to conserve power without creating an impedance too weak to drive the ADC input.

9.2.1.2.6 Input Filtering

The MSP430 ADC is configured to run from the 1.1-MHz SMCLK with an oversampling rate (OSR) of 256, yielding a sample rate of roughly 4.3 kHz. The input filter cutoff frequency is set to 1 kHz in order to limit the input signal bandwidth, as shown in Equation 17. R_8 is 1 kΩ in order to provide isolation from the capacitive load of the low-pass filter, thereby reducing stability concerns.

$$f_{-3dB_A1+} = 1\ \text{kHz} = \frac{1}{2 \cdot \pi \cdot R_8 \cdot C_1}$$

where

- $C_1 = \dfrac{1}{2 \cdot \pi \cdot 1\ \text{k}\Omega \cdot 1\ \text{kHz}} = 159\ \text{nF}$ (17)

Reduce C_1 to 150 nF so that it is a standard value.

The A1– input of the delta-sigma (ΔΣ) converter is not buffered, and therefore requires a large capacitor to supply the charge for the internal sampling capacitor. A 47-µF capacitor is selected, resulting in the cutoff frequency illustrated in Equation 18.

$$f_{-3dB_A1-} = \frac{1}{2 \cdot \pi \cdot \left(\frac{R_6}{2}\right) \cdot C_2} = 0.144\ \text{Hz} \tag{18}$$

In applications that cannot tolerate such a low-frequency cutoff, and therefore a long start-up time, buffer the A1– input with another OPA317 to properly drive the ADC input with a lower-input capacitor.

9.2.1.2.7 Passive Component Tolerances and Materials

Resistors R_1, R_2, R_3, R_4, R_5, R_6, and R_7 directly affect the accuracy of the circuit. To meet the unadjusted accuracy goals of 0.2%, the resistors used are 0.1%. Select 0.1% resistors for the construction of the difference amplifier circuit to provide a common-mode rejection ratio (CMRR) of at least 60 dB.

9.2.1.3 Application Curves

9.2.1.3.1 DC Performance

The measured dc performance and calculated error of the circuit is shown in Figure 20 and Figure 21, respectively. By applying a two-point gain and offset calibration over the specified ±5-V input range, the calibrated error is shown in Figure 22. The uncalibrated results show errors of 138 μV, or 0.0138%FSR. The calibrated results with a simple two-point calibration show errors under 5 μV, or 0.0005%FSR, in the specified input range of ±5 V.

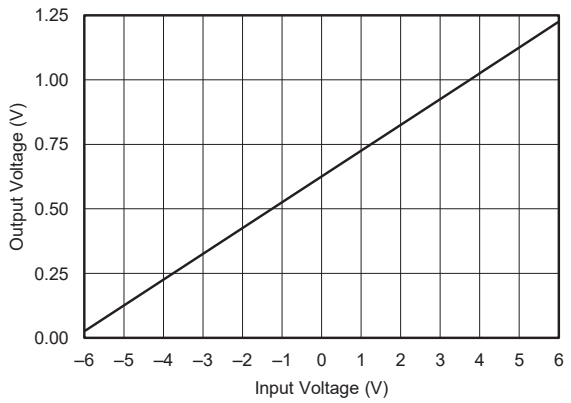


Figure 20. Measured DC Transfer Function with ±6-V Input

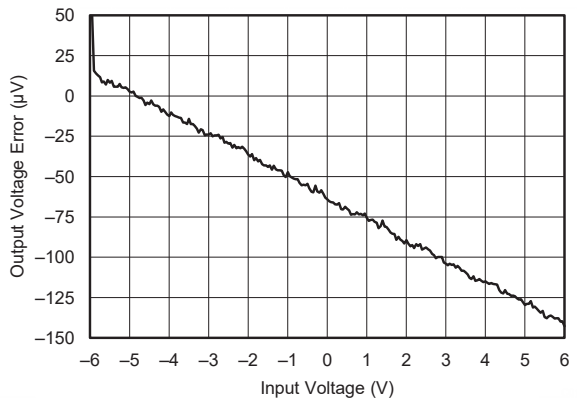


Figure 21. Measured Output Error with ±6-V Input

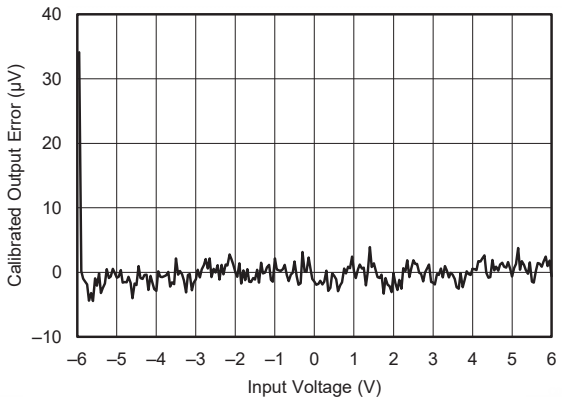


Figure 22. Calibrated Output Error with ±6-V Input

9.2.1.3.2 AC Performance

The ac transfer function for the attenuation and level-shifting circuit is shown in Figure 23.

The low-frequency ac CMRR performance is measured to be 62 dB, as shown in Figure 24.

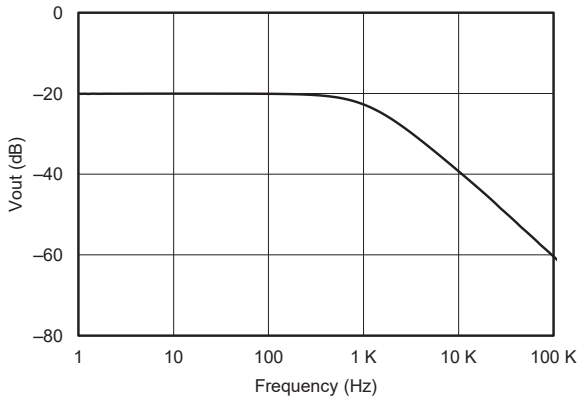


Figure 23. Measured AC Transfer Function

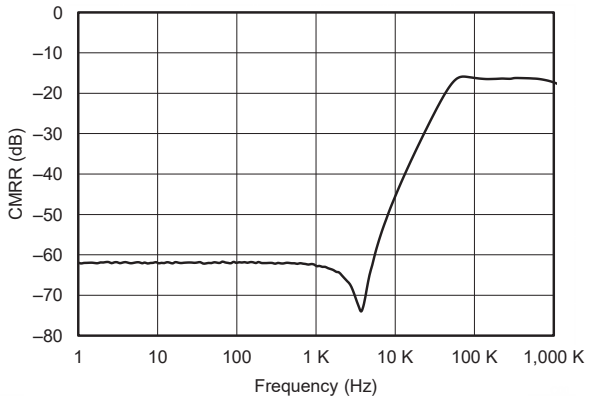


Figure 24. Measured AC CMRR Results

10 Power-Supply Recommendations

The ZCC33xx family of voltage references features extremely low dropout voltage, except for the ZCC3312. The ZCC3312 has a minimum supply requirement of 1.7 V. These references can be operated with a supply 110 mV above the output voltage with a 5-mA load (typical). For loaded conditions, a typical dropout voltage versus load graph is illustrated in Figure 4 of the *Typical Characteristics*.

If the supply voltage connected to the IN pin is rapidly moved when the ZCC33xx is connected to a capacitive load, a reverse voltage can discharge through the OUT pin and into the ZCC33xx. This voltage does not damage the ZCC33xx, provided that the voltage is less than or equal to 5 V.

11 Layout

11.1 Layout Guidelines

For optimal performance of this design, follow standard printed circuit board (PCB) layout guidelines, including proper decoupling close to all integrated circuits and adequate power and ground connections with large copper pours. Select a PCB size with connectors that connect directly to the MSP430 LaunchPad™.

Figure 25 shows an example of a PCB layout for a data acquisition system using the ZCC33xx.

Some key considerations are:

- Connect a low-ESR, 1-µF ceramic capacitor at the IN pin for bypass, and a 0.1-µF to 10-µF ceramic capacitor at the OUT pin for stability of the ZCC33xx.
- Decouple other active devices in the system per the device specifications.
- Use a solid ground plane helps distribute heat and reduces EMI noise pickup.
- Place the external components as close to the device as possible. This configuration prevents parasitic errors (such as the Seebeck effect) from occurring.
- Minimize trace length between the reference and bias connections to the ADC to reduce noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when absolutely necessary.

11.2 Layout Example

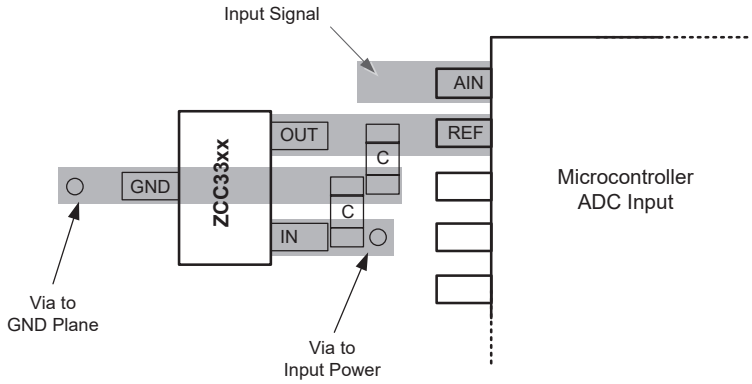
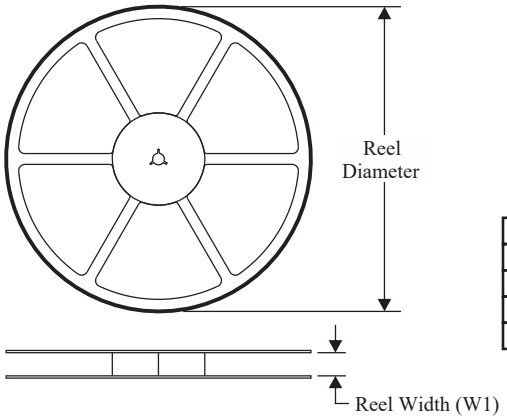


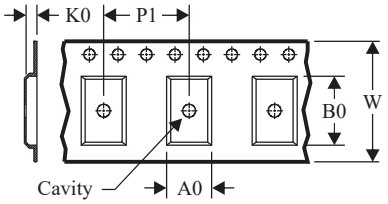
Figure 25. Layout Example

TAPE AND REEL INFORMATION

REEL DIMENSIONS

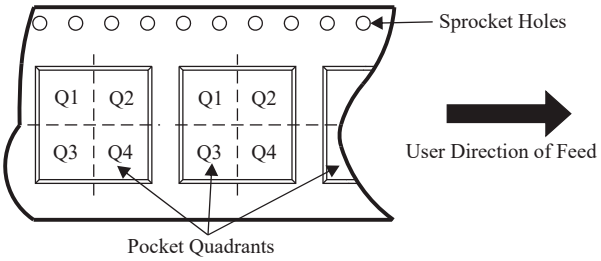


TAPE DIMENSIONS



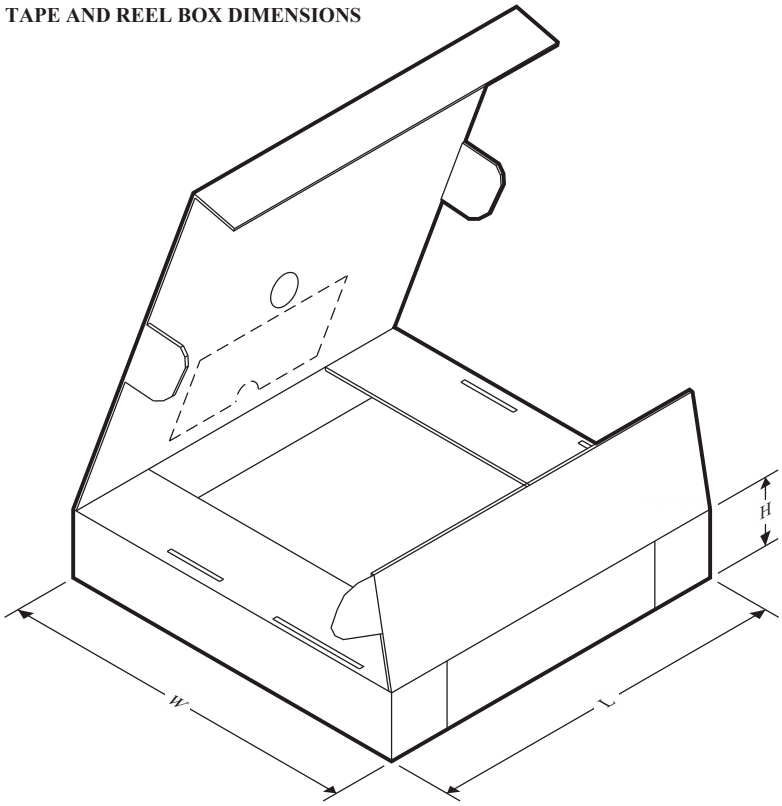
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

TAPE AND REEL BOX DIMENSIONS

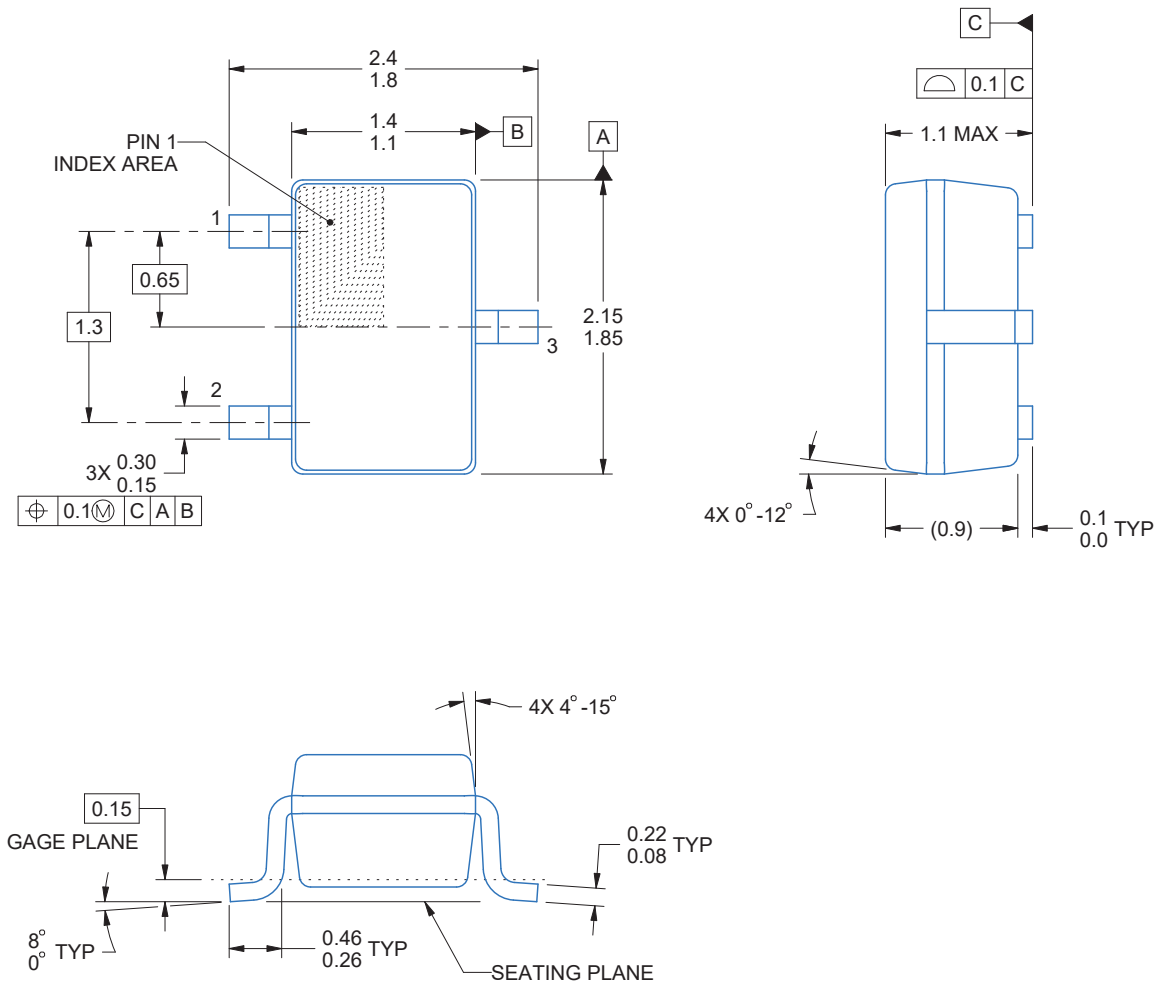


*All dimensions are nominal

PACKAGE OUTLINE

SOT-SC70 - 1.1 max height

SMALL OUTLINE TRANSISTOR SC70



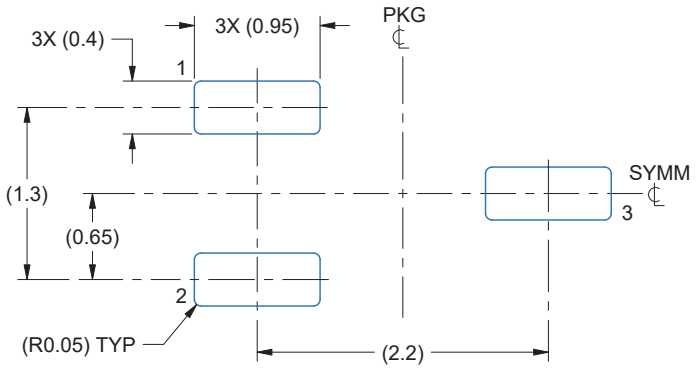
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

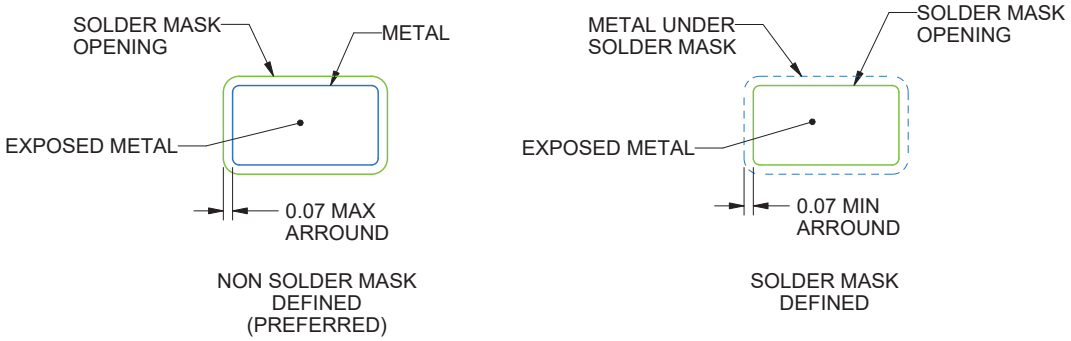
EXAMPLE BOARD LAYOUT

SOT-SC70 - 1.1 max height

SMALL OUTLINE TRANSISTOR SC70



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



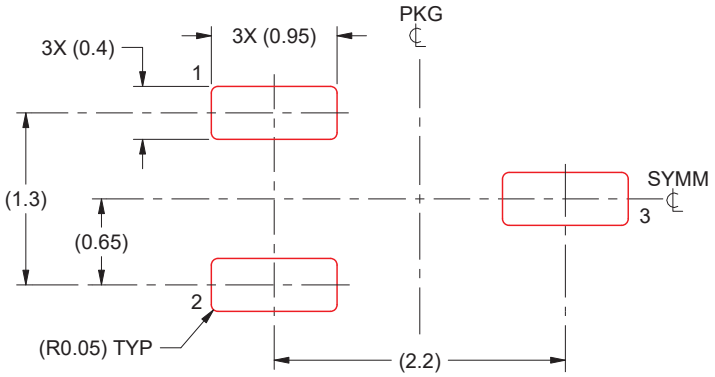
SOLDER MASK DETAILS

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

SOT-SC70 - 1.1 max height



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

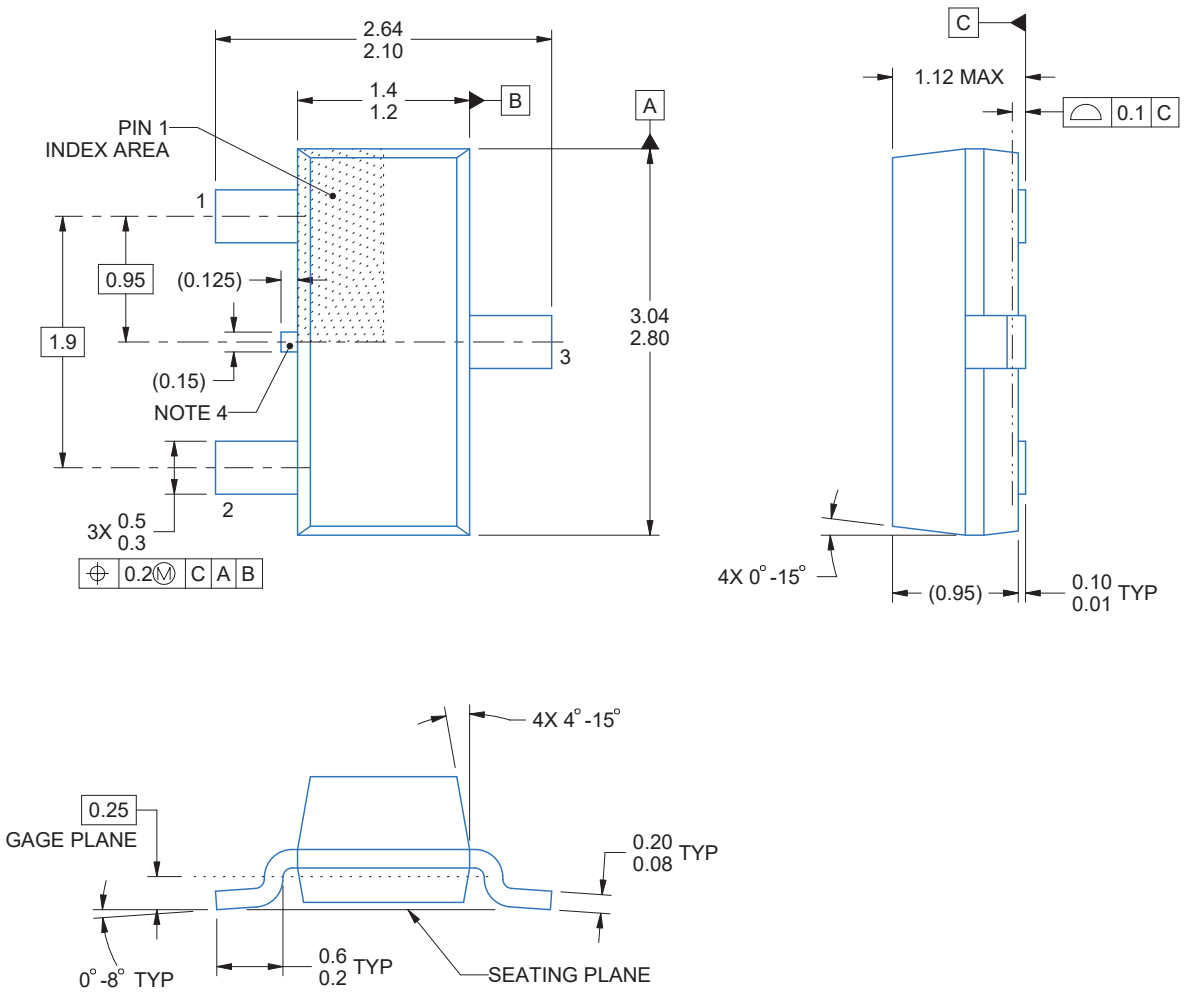
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



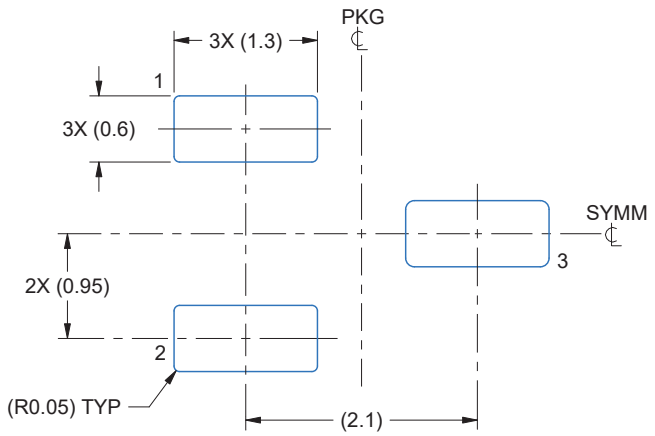
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.
4. Support pin may differ or may not be present.
5. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

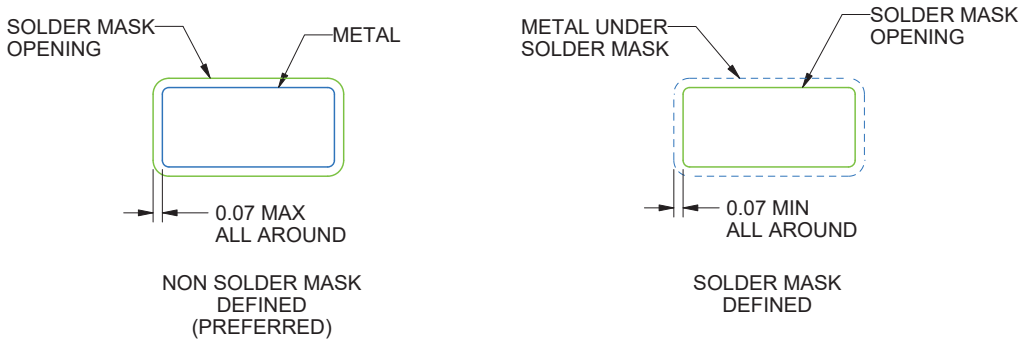
EXAMPLE BOARD LAYOUT

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

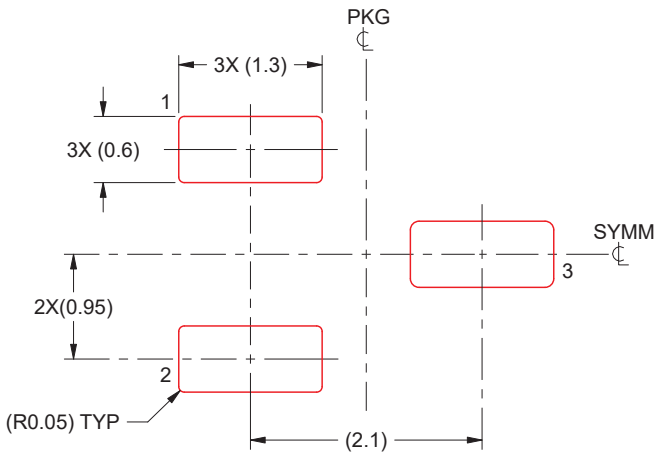
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

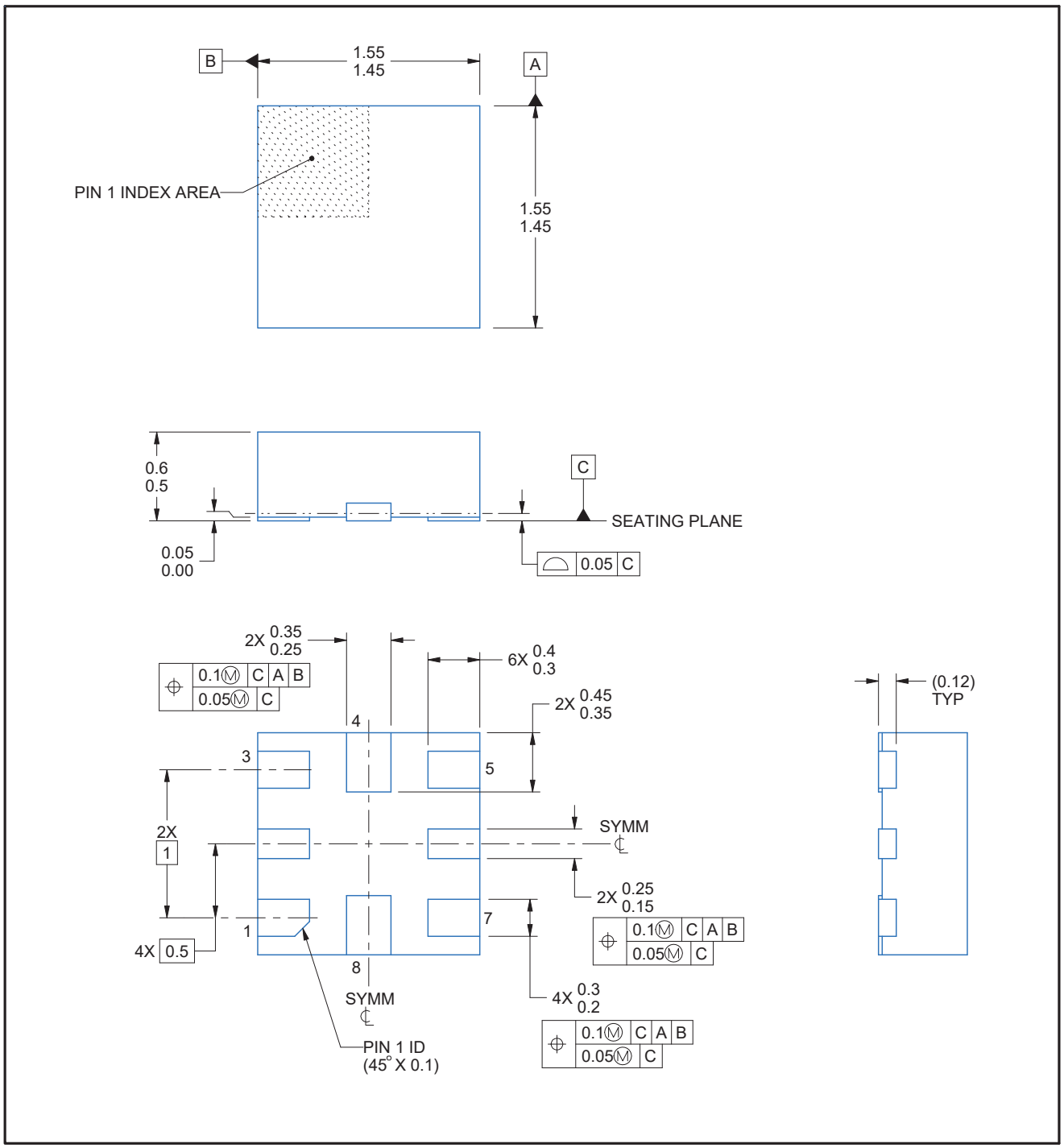
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

UQFN - 0.6 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



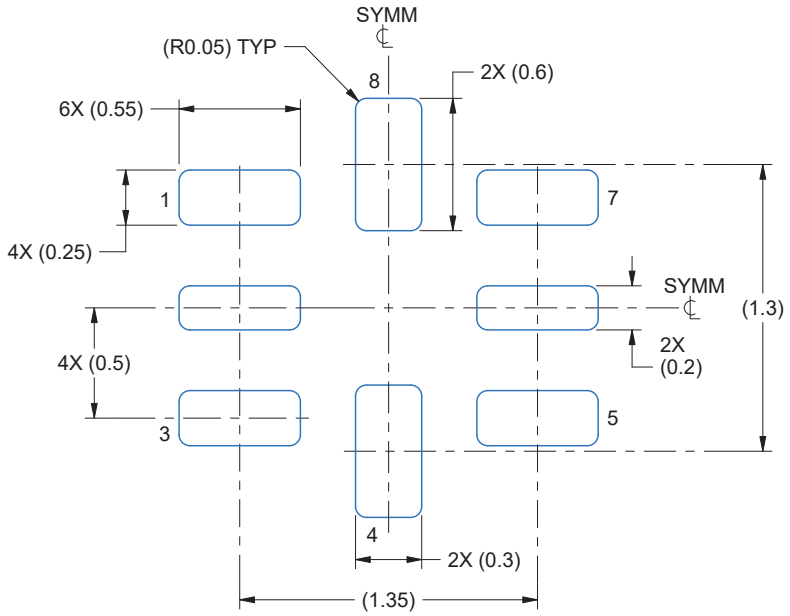
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

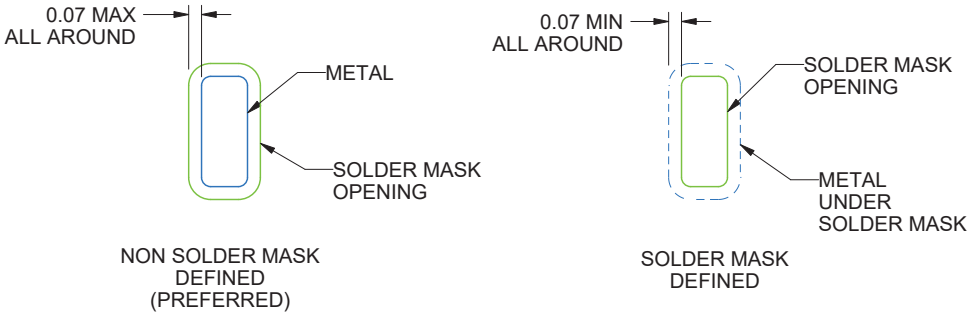
EXAMPLE BOARD LAYOUT

UQFN - 0.6 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:30X

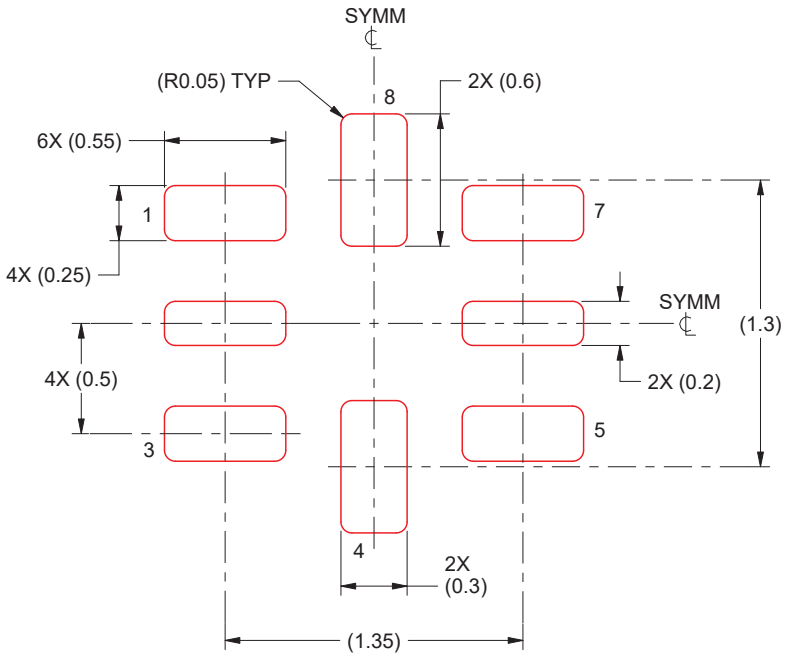


SOLDER MASK DETAILS
NOT TO SCALE

EXAMPLE STENCIL DESIGN

UQFN - 0.6 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICKNESS
SCALE: 30X

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.